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Fabrication of $Cu_2ZnSnSe_4$ Thin-film Solar Cells by a Two-stage Process

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Fabrication of $Cu_2ZnSnSe_4$ Thin-film Solar Cells by a Two-stage Process

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
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DEDICATION

This dissertation is dedicated to everyone who has helped me through my PhD study.

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I would like to thank my major professor Dr. Don Morel for his continuous guidance and support throughout my entire PhD study. I really appreciate his mentorship and instruction. And also I would like to express my gratitude to Dr. Christos Ferekides for his great help and support. Furthermore, I would like to thank all the members of III-V semiconductor lab at University of South Florida for their help.

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ABSTRACT

Copper zinc tin selenide ($Cu_2ZnSnSe_4$ or CZTSe) is a quaternary compound semiconductor material that has attained more and more attention for thin film photovoltaic applications. CZTSe is only comprised of abundant and non-toxic elements. People have concerns about availability and cost of indium from CIGS and tellurium from CdTe, also about cadmium's toxicity. These concerns have promoted CZTSe as an alternative thin film solar cell material. The major issues about CZTSe absorber fabrication are: tin loss during selenization process and existence of secondary phases. Recent improvements of CZTSe absorber have increased the efficiency of CZTSe thin film solar cell to 9.7% in laboratory, and this was accomplished by using H_2Se as selenium source in a "two-stage" process. [1] However "one-stage" vacuum co-evaporation technique is still the most popular technique for CZTSe thin-film solar cells fabrication.

In this research, $Cu_2ZnSnSe_4$ thin-film solar cells have been fabricated by using a two-step rapid thermal selenization process. The first step selenization is operated at 375℃, a relatively low annealing temperature, which helps avoiding the most common issue of tin loss. The second step selenization is carried out at a higher annealing temperature, 400℃ to 500℃, at where the formation of CZTSe quaternary compound can be completed, and fewer secondary phases remain in the CZTSe absorber bulk. A specially designed metallic precursor stacks deposition order has been developed to inhibit tin loss and zinc loss during selenization. Vacuum co-evaporation technique is not feasible to mass production, due to facility difficulty and bad uniformity. And H_2Se is toxic and dangerous. We have developed these metallic precursor stacks

vacuum deposition process and two-step selenium vapor selenization process. We believe this technique is more suitable for potential mass production in future.

The properties of CZTSe thin-films and the performance of CZTSe thin-film solar cells have been characterized using techniques, including J-V, Raman spectroscopy, spectral response, and SEM/EDS. The best performance CZTSe thin-film solar cell that have been accomplished, has an open circuit voltage of 0.42 volt, shirt circuit current densities of 14.5 mA/cm^2, fill factor of 47%, and efficiency of 2.86%.

CHAPTER 1: INTRODUCTION

The International Energy Agency, predicted the world electricity generation is increasing from 20.2 trillion kilowatt-hours in 2010 to 39.0 trillion kilowatt-hours in 2040. [2] Worldwide energy security concern and climate change caused by greenhouse gas emissions have provoked extensive international policies and laws that promote a persistent increasing investment on sustainable energy technologies. As a result, renewable energy sources will become the fastest growing electricity power generation sources from 2010 to 2040 at around 2.8 percent per year. [2]

The International Energy Agency also predicts that photovoltaic solar technologies generated electricity production would contribute about 17 percent of overall global clean electricity production and 20 percent of all renewable electricity generation by 2050. [2] Solar photovoltaic generated electricity costs keep dropping for years since the beginning of 1990s and are expected to meet the fossil fuel generated electricity costs by 2030. The photovoltaic system installment capacity is predicted to be 1.5-2.5 TWh (terawatt-hours) by 2030, in which 35% of solar photovoltaic industry is taken by thin-film photovoltaic solar panels. [3]

Thin-film solar cells are manufactured by depositing or growing layers of thin (nm to μm) semiconducting materials onto substrates. The substrates of thin-film solar cells can be glass, polymer and stainless steel. At present, commercialized thin-film solar cell materials are including amorphous thin-film silicon (a-Si), cadmium telluride (CdTe), copper indium gallium diselenide (CIGS), and gallium arsenide (GaAs). Compared to crystalline silicon solar cells (c-

Si), which have a normal wafer thickness of up to 200 μm, thin film semiconductor materials allow thin film solar panels to be flexible, lower weight, less materials consuming, and lower costs.

However, concerns have been raised on the availability of thin-film semiconducting materials for rapid growth of thin-film photovoltaic production. For instance, for CdSe thin film solar cells, there have been concerns about tellurium's cost and availability. And cadmium's toxicity presented in both cadmium sulfide and cadmium telluride is also an environmental concern. For gallium arsenide, the environmental toxicity risks associated with arsenic may also restrict its extensive application. For copper indium gallium (di)selenide (CIGS) thin-film technologies, there are also concerns about materials availability of gallium and indium. The material mass productions of gallium, indium, and tellurium are minor byproducts of aluminum production, zinc production, copper production, and lead production. [5] 2010 U.S. Department of Energy report has claimed these three elements as critical, and indium is evaluated as the highest criticality in a short term. [5] All of these concerns over availability and toxicity of materials have driven new thin film technology research to discover new alternative thin film semiconductor absorbers made from environmentally friendly, low cost and earth abundant materials.

CZTS family, which is only based on abundant and non-toxic elements, has attracted more and more attention as a promising thin film semiconductor material in solar photovoltaic application. CZTS, or $Cu_2ZnSn(S, Se)_4$, is a relatively new quaternary kesterite structure compound semiconducting material. The CZTS family of related materials includes copper zinc tin sulfide (CZTS), copper zinc tin selenide (CZTSe), and sulfur/selenium alloy CZTSSe. The band gap of Cu_2ZnSnS_4 is 1.40-1.50 eV, while the band gap of $Cu_2ZnSnSe_4$ is 0.9-1.0 eV and the band gap

of $Cu_2ZnSn(S_x, Se_{(1-x)})_4$ is between 1.0 eV and 1.5 eV. [6] They are close to 1.35 eV, the best band gap required by semiconductor in solar cell application. [7] Kesterite structure of CZTS is similar to the chalcopyrite structure of CIGS. However CZTS only uses low cost and earth abundant elements. Raw materials used for CZTS are around five times cheaper than CIGS. [2] Evaluations of global material reserves for Copper, Tin, Zinc, and Sulfur, indicate that only 0.1% of worldwide available raw material resources could supply the total energy consumption of the whole world. [12] CZTS is a semiconductor material with a direct band gap and a high absorption coefficient of over 10^4 cm^{-1}. [13] Hence as a non-toxic and earth-abundant thin-film absorber, CZTS has become a promising candidate for the thin film solar cell absorber layer.

Multifarious fabrication methods have been developed for CZTS thin film solar cells fabrication, including physical methods such as thermal evaporation, pulsed laser deposition, spray pyrolysis technique, ultrasonic spray pyrolysis, atom beam sputtering, electro-deposition; and chemical methods such as, sol-gel, spin coating technique, hot injection, hydrothermal, and SILAR technique. [8]

Japanese thin film solar cell company Solar Frontier reported a world record CZTSSe solar cell with a12.6% energy conversion efficiency has been developed by a chemical solution approach using hydrazine as a solvent in 2013. [9] And an efficiency of 9.15% has been accomplished for CZTSe thin film solar cells by using physical fabrication method. [10] Hydrazine is a colorless, flammable, hazardous, highly toxic, explosive and dangerously unstable liquid. Therefore, the chemical fabrication method using hydrazine is not feasible for solar panel mass manufacturing process. Physical fabrication methods have the advantage to overcome problems coming with chemical methods, such as time-consuming, hazardousness, poor uniformity and crystallinity. Physical methods also have weaknesses, such as high costs of high vacuum equipments and

complicated maintenance. While the advantages of physical methods are including, better crystallinity, simple-control on structure and morphology of thin film layers, simple-control on thin film deposition. [4] [11]

CHAPTER 2: SOLAR CELL DEVICE PHYSICS

Solar cell is semiconductor device which transforms solar radiant energy directly into electrical energy. When electrons from the semiconductor material absorbers in solar cell devices receive energy of incident photons and obtain energy equal to the band-gap of the semiconductor material, they become excited, transfer from valence band to conduction band, and then they become free to move around the semiconductor and participate in conduction. In this way, a solar cell device converts the incident photon energy into the energy of electrons. Photons with energy lower than the solar cell semiconductor band-gap cannot excite any electron out of valence band in semiconductor material, hence they cannot be absorbed by the semiconductor.

As input photons are absorbed and obtained by the semiconductor absorber of solar cell, electron-hole pairs are created across P-N junction. However, electrons created at the P-type semiconductor side and holes created at the N-type semiconductor side can only exist for a time length of minority carrier lifetime in the material before they recombine together. Once the carriers recombine, the generated electron-hole pairs are gone, so they cannot contribute to current collection anymore.

However the presence of a P-N junction impedes this carrier recombination by separating holes and electrons towards different directions in the electric field within the P-N junction. If these carriers reach the P-N junction, then they are collected across the junction area by the existing electric field across the junction. In this way, carriers are collected across the P-N junction area and become majority carriers. If the front contact and back contact of the solar cell device are

connected together short-circuited or through an external load, then these carriers could flow across the external circuit, known as light-generated current. [14]

2.1 Semiconductor

In solid-state physics textbook, a semiconductor is defined as a material, which has an electrical resistivity in the scope of $10^{-2} – 10^{9}$ Ω·m. It also can be defined as a material, which has an electronic excitation energy band gap standing between 0 and around 4 electron volts. Semiconductors are the foundation of modern electronics industry. [15]

Semiconductor materials could have various different chemical compositions and crystal structures. There are elemental semiconductors, such as Silicon, Selenium, and Carbon(C_{60} or nanotubes); and compound semiconductors, such as gallium arsenide (GaAs), cadmium telluride (CdTe), indium gallium arsenide (InGaAs), and copper indium gallium di-selenide (CIGS). [15]

The conductivity of semiconductors can be modified by doping impurities in the semiconductor's crystal lattice. The process of doping is to intentionally add controlled amount of impurities to the structure of an intrinsic semiconductor. An intrinsic semiconductor is a pure semiconductor. In an intrinsic semiconductor, there are thermal excitation created free electrons at the conduction band and thermal excitation created free holes at valence band. For a doped semiconductor, impurities are introduced into its crystal lattice, and holes or electrons are supplied by dopant atoms acting as an impurity in crystal lattice. By doping impurities, the conductivity of doped semiconductors can be varied by factors of millions. When a semiconductor has a high level of doping, and the semiconductor acts more like a metal, it becomes a degenerate semiconductor. [15]

In a semiconductor material, “band-gap” is defined as the energy difference between the top of the valence band and the bottom of the conduction band. Since there is no allowed energy states within the band-gap, electrons can only jump from one band to the other. A minimum amount of energy, which is equal to the band-gap energy, is required for an electron to transfer from valence band to conduction band. And the bang-gap of semiconductors decreases as temperature increases. The relationship between band-gap energy of semiconductor and temperature of semiconductor is given by Varshni empirical expression:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta}$$, while α and β are material constants.

Depending on the electronic band structure, there are two types of band gaps, direct band gap and indirect band gap. For an indirect band gap semiconductor, an electron transition from valence band to the conduction band requires a change of momentum. While for a direct band gap semiconductor, it does not require such a momentum change. And in an indirect semiconductor, a change of momentum is required for an electron transition. [15][16]

2.2 P-N Junction

There are two types of extrinsic semiconductor: N-type and P-type. N-type semiconductor is created by doping an intrinsic semiconductor with donor impurities. So N-type semiconductor has a larger electron concentration than hole concentration. The “n-type” means the “negative” charge of the electron. In N-type semiconductor, the dopant atoms provide extra conduction electrons to the intrinsic material, and create an excess of n-type electron charge carriers. In N-type semiconductors, electrons are the majority carriers, while holes are the minority carriers. For instance, N-type silicon can be created by doping phosphorus as figure 1 in below. In n-type

semiconductors, the Fermi level of n-type semiconductor stays closer to the conduction band than the valence band, and it is greater than the Fermi level of the intrinsic semiconductor. [15]

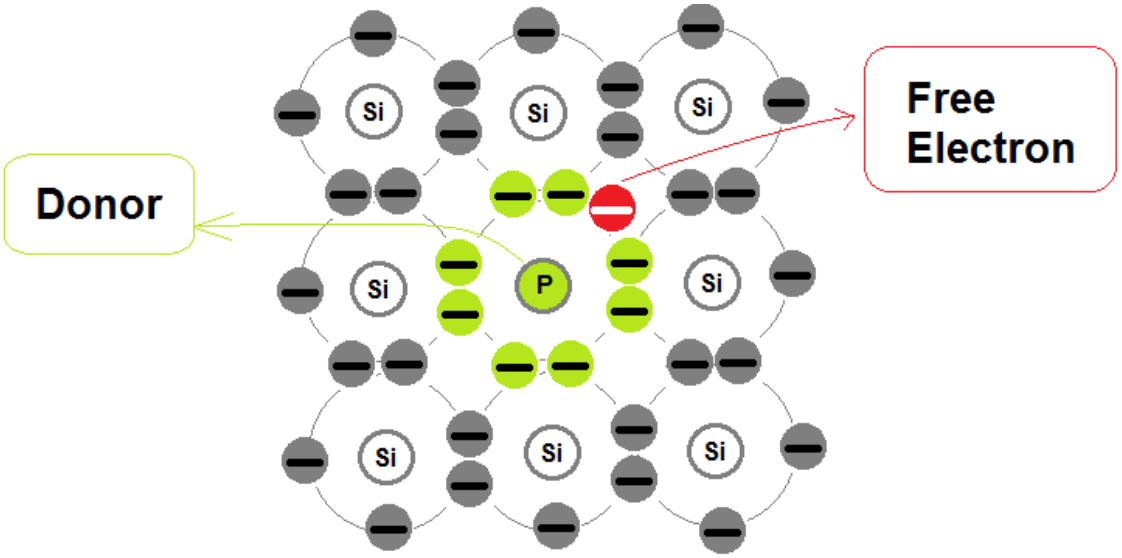

Figure 1 N-type semiconductor (phosphorus in silicon)

In P-type semiconductors, there are a larger hole concentration than electron concentration. "P-type" comes from the "positive" charge of the hole carriers, which are the majority carriers, while electrons are the minority carriers. P-type semiconductors are produced by doping acceptor impurities into intrinsic semiconductors. For instance, P-type silicon can be created by doping boron, as shown in figure 2. The dopant boron atom accepts an electron, leading to lose half bond to its neighboring atom, which causes forming a hole. Each hole is related with a nearby charged boron ion, so that the semiconductor remains neutral as a unit electrically. However, when a hole has drifted away in the lattice, it is positively charged and it behaves as a unit of positive charge. If a large amount of acceptor atoms are doped into an intrinsic semiconductor, the holes outnumber the thermally excited electrons significantly, and holes become the majority

carriers in the semiconductor. For P-type semiconductors, the Fermi level stays closer to valence band than conduction band, and it is below the intrinsic Fermi level. [15]

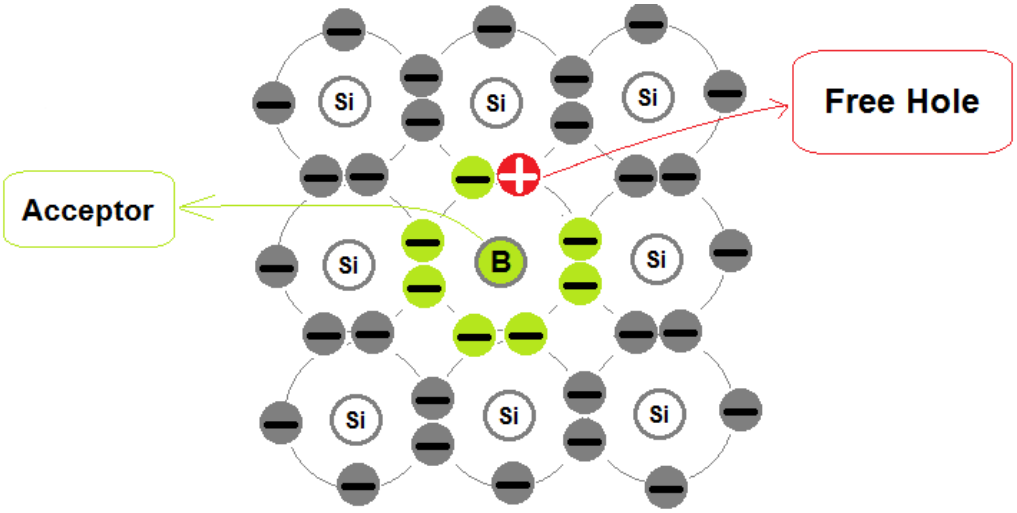

Figure 2 P-type semiconductor (boron in silicon)

P-N junctions serve an important role in modern electronic industrial applications. It has been widely used in rectification, switching, and other electronic circuit operations. [17] It is also the building block of many semiconductor electronic devices, such as bipolar transistors, thyristors, diodes, LEDs, solar cells, integrated circuits, and metal oxide semiconductor field effect transistors. [18]

A P–N junction is a two-terminal device, including a N-type semiconductor terminal and a P-type semiconductor terminal. And the P-N junction is formed at the interface between these two types of semiconductor materials. When the P-type and N-type semiconductors are jointed together, the carrier concentration gradients at the P-N junction interface cause carriers diffusion. Holes from the P-type terminal diffuse into the N-type terminal, while electrons from the N-type terminal diffuse into P-type terminal. Hence, diffusion current $J_{diffusion}$ flows from the P-type

semiconductor terminal to the N-type semiconductor terminal. The formation of diffusion current is created by the carrier concentration gradients at the P-N junction interface. As the diffusion of holes leave the P-type semiconductor terminal, the negative acceptor ions around the P-N junction are left uncompensated, because the acceptors are fixed in the lattice, whereas holes are mobile carriers. On the other hand, as the electrons flow into the P-type semiconductor terminal from the N-type semiconductor terminal, some of the positive donor ions around the P-N junction are left uncompensated. Consequently, a negative charged area forms around the P-type terminal, and a positive charged area forms near the N-type terminal. So an electrical field is formed, and its direction is from the positive charged N-type terminal to negative charged P-type terminal, as shown in figure 3 as below.

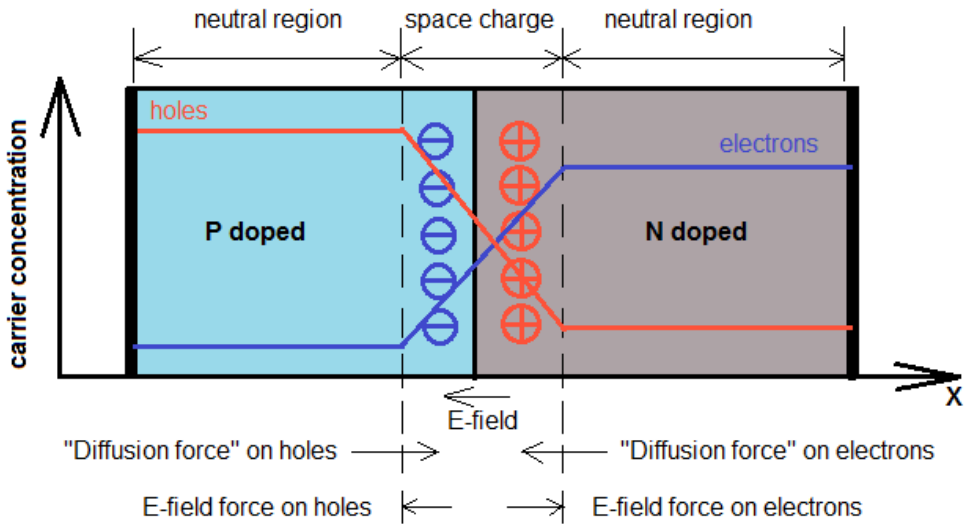

Figure 3 Zero-bias voltage applied P-N junction in thermal equilibrium

A depletion layer is formed at the region nearby the P-N junction interface. Because this region becomes charged, it forms a space charge zone. The built-in electric field is in the direction opposite to the direction of diffusion current. So in a P-N junction, without an external applied voltage bias, it reaches an equilibrium condition. And a potential difference is formed across the

P-N junction area, and we name this potential difference as "built-in" potential V_{bi}. [18] The electric field created in depletion layer opposes the diffusion current. This diffusion current generates more space charges in the depletion layer, and the electric field created by the space charge counters the diffusion current until an equilibrium is established in the depletion layer. [18] At the thermal equilibrium, the current flowing across the depletion layer is zero. Hence the carrier drift current due to the electric field exactly counters the diffusion current produced by the carrier concentration gradient. This electrostatic potential difference between the P side and the N side at the thermal equilibrium is we called the "build-in" potential V_{bi}. Energy band diagram of a p-n junction is shown in figure 4 as below.

$$V_{bi} = \psi_n - \psi_p = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

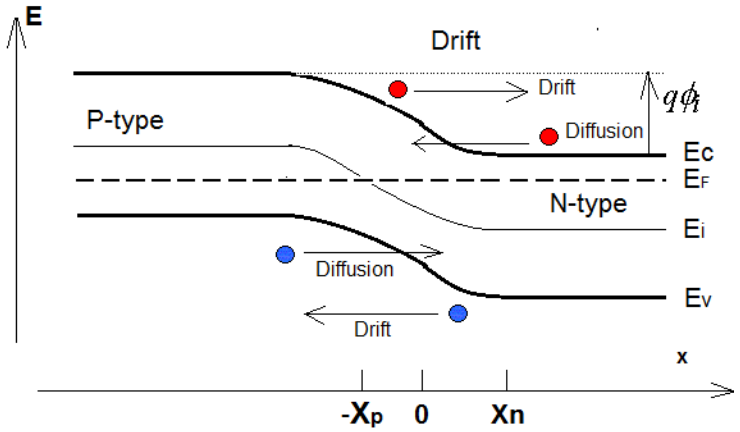

Figure 4 P-N junction energy band diagram in thermal equilibrium

In figure 5, it shows the diagrams of charge density, electric field and voltage, when a P-N junction is in at thermal equilibrium with zero bias.

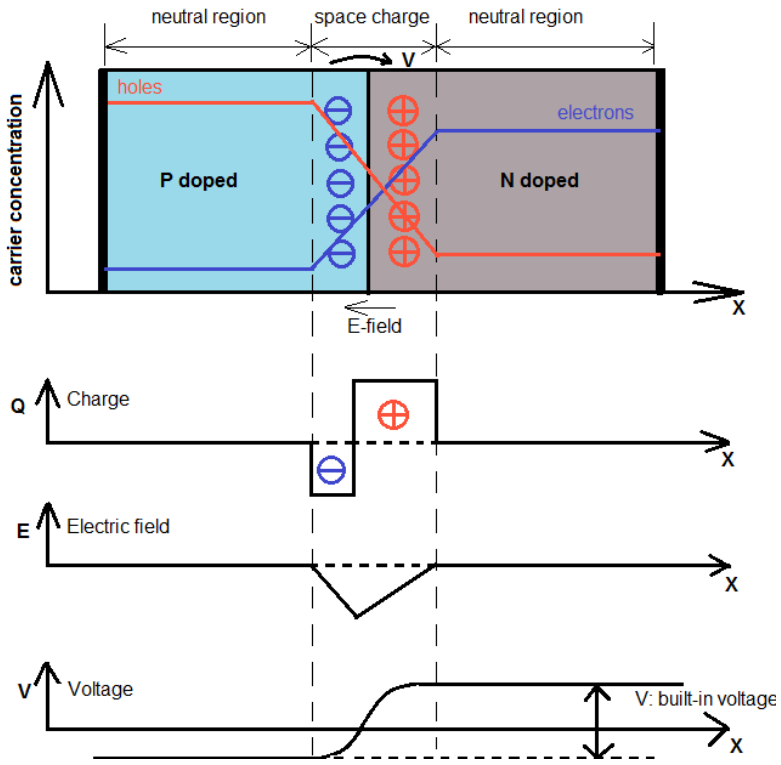

Figure 5 P-N junction at thermal equilibrium and zero bias, charge density, electric field and voltage diagrams

In forward bias mode of P-N junction, the p-type side is connected to positive terminal and the n-type is connected to negative terminal. When a P-N junction is in forward-bias operation condition, the width of the depletion layer is reduced. The positive potential applied onto the p-type end repels holes, as the negative potential applied onto the n-type end repels electrons. As holes from p-type side and electrons from n-type are pushed to the P-N junction interface, the width of depletion layer is reduced. [15] [18]

In reverse bias mode of P-N junction, the p-type end is connected with the negative terminal of power source and the n-type end is connected to the positive terminal of power source. The holes in the p-type material are dragged away from the P-N junction, resulting in increasing of the width of depletion zone. Likewise, the electrons will also be dragged away from the P-N

junction. So the depletion region becomes widen, and extends with increasing reverse-bias voltage. And no current flows until the P-N junction breaks down due to the reverse-bias. [18]

2.3 Heterojunction

A heterojunction is the junction formed between two regions of dissimilar semiconductors. These semiconducter materials have unequal band gaps E_g, and different dielectric permittivities ε_s, different work functions $q\phi_s$, and different electron affinities $q\chi$. The difference in energy of the conduction bands in the two semiconductors is represented by ΔEc, and the difference in energy of the valence bands is represented by ΔEv. [19]

$$\Delta Ec = q\,(\chi_2 - \chi_1)$$

$$\Delta Ev = \Delta Eg - \Delta Ec$$

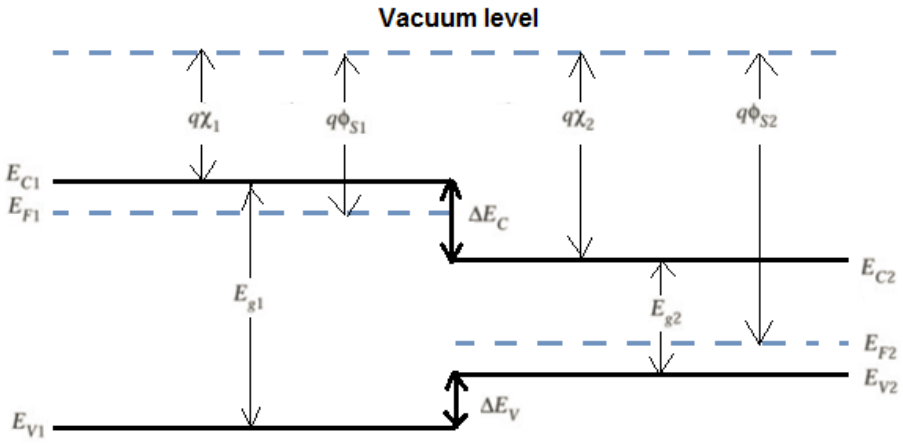

Figure 6 Energy band diagram of two dissimilar isolated semiconductors

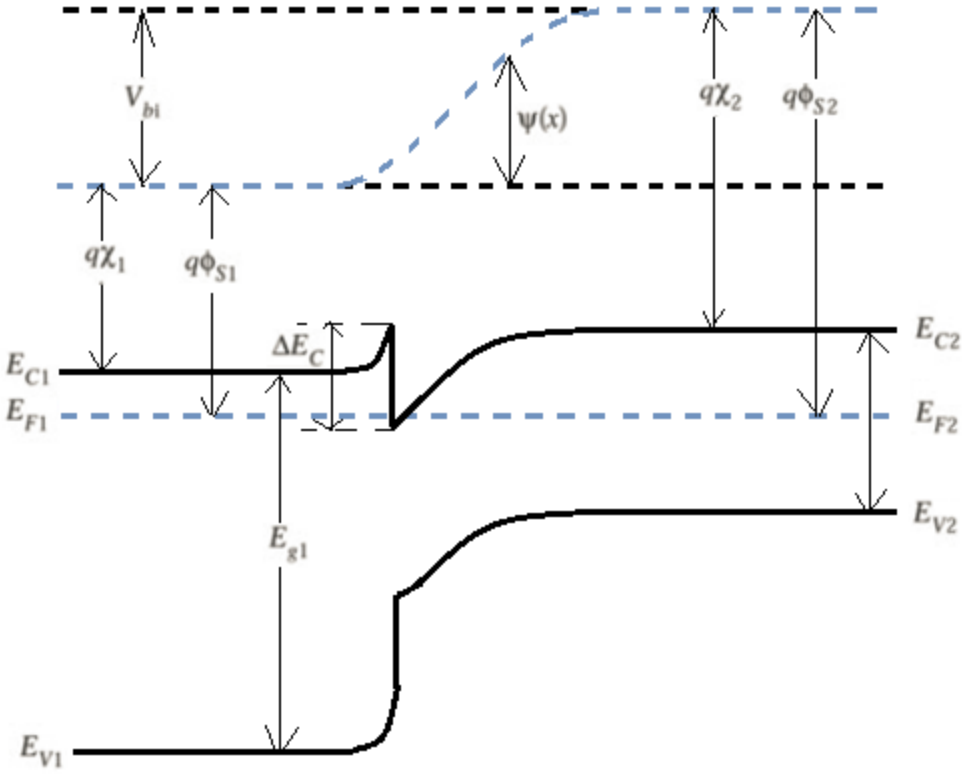

Figure 7 Energy band diagram of an ideal n-p heterojunction at thermal equilibrium

In figure 6, energy band diagram of two isolated dissimilar semiconductors are shown. In figure 7, the equilibrium band diagram of an ideal abrupt heterojunction formed between two dissimilar semiconductors. There are two basic requirements in the constructions of the energy band diagram: [20]

1). In thermal equilibrium, the Fermi level must be the same at the both sides of interface.

2). The vacuum level is continuous, and it is parallel to band edges. The total built-in potential V_{bi} can be expressed by:

$$\boldsymbol{V_{bi} = V_{b1} + V_{b2}}$$

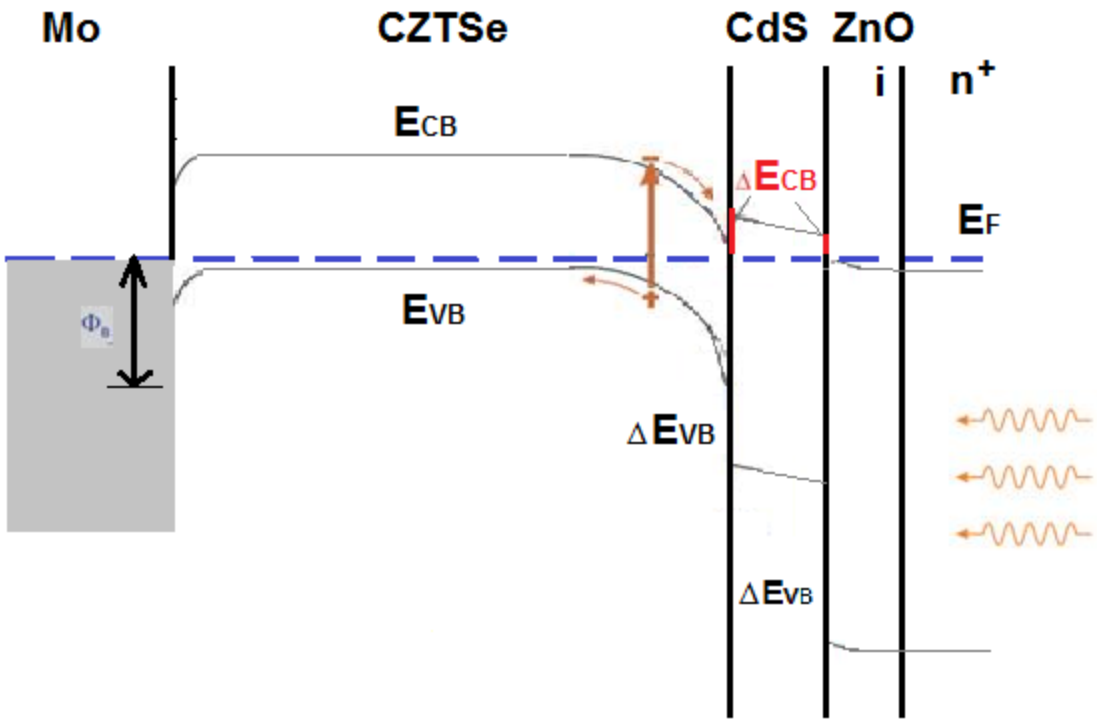

Figure 8 CZTSe energy band diagram

In the research of CZTSe thin-film solar cell, CZTSe thin-film device is a hetero-structure. The charge carrier generation happens in the CZTSe absorber bulk, and it is caused by the incident light. The generated electrons are moved to conduction band. The electrons are transported to the CdS layer, due to the band bending. The holes in valence band are transited to the molybdenum back contact. The different barriers (ΔE_{VB} and ΔE_{CB}) across the interfaces between the materials need to be as low as possible, so that a charge transportation could take place in the conduction and valence band.

2.4 Metal Semiconductor Contacts

In solar cell devices, a metal semiconductor contact is a type of junction in which a metal material is in contact with a semiconductor material. Metal semiconductor contact can be rectifying, the rectifying metal-semiconductor junction can form a Schottky barrier. And metal-

semiconductor contact can also be non-rectifying. The non-rectifying junction is also called ohmic contact. The formation of ohmic contacts is desirable for better thin film solar cell performance, because electrical charges can be conducted easily between the active regions of semiconductor absorber bulk and the back contact metal. [20]

2.4.1 Ohmic Contact

An ohmic contact is a metal semiconductor contact, which has a negligible contact resistance relative to the bulk resistance of the semiconductor. The contact resistance of an ohmic contact is independent of the applied voltage, and is so small that charge carriers could flow freely through the semiconductor. Ohmic contacts are critical to the performance of any high-current device. [21]

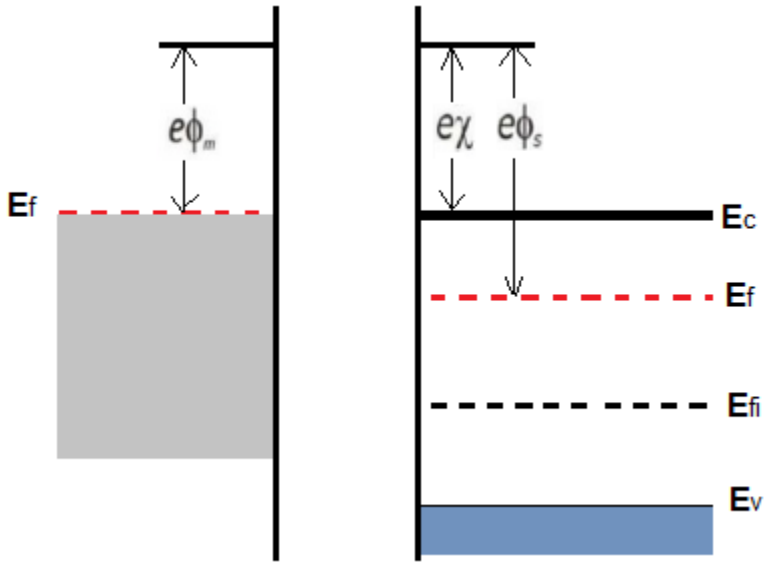

Figure 9 Energy band diagrams of a metal adjacent to a N-type semiconductor

Figure 9 shows the energy band diagram of a metal and a N-type semiconductor. And the work function of metal, Φ_M, which is less than the work function of N-type semiconductor, Φ_S. When the metal and the semiconductor have formed a contact, electrons flow from metal to

semiconductor, and the Fermi levels line up. [21] And the bands in the semiconductor side bend down, no depletion layer is created. The electrons can flow freely from the semiconductor side to the metal side, since there is no barrier left. Energy band diagram of a metal N-type semiconductor in equilibrium is shown in figure 10.

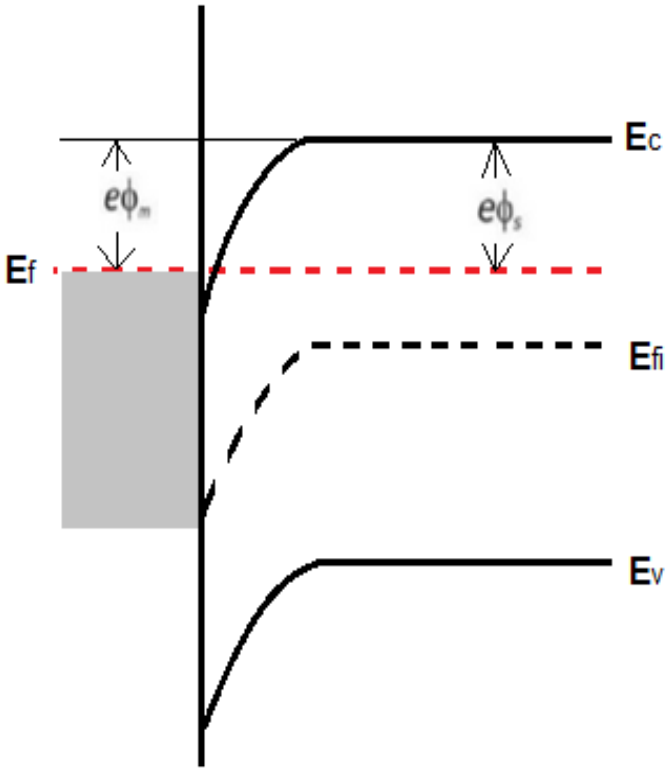

Figure 10 Energy band diagram of a metal and N-type semiconductor contact in thermal equilibrium

2.5 Solar Cells

A solar cell is a semiconductor electrical device that converts the energy of incident solar radiation directly into electrical energy. In a solar cell, incident photons are absorbed to generate electron-hole pair charge carriers that can pass through an external load to do electrical work. Solar cell is a semiconductor photovoltaic device. [22]

2.5.1 Solar Radiation

The solar radiation energy from the sun derives from the nuclear fusion reaction inside the sun, where 6×10^{11} kg hydrogen is converted to helium every second with an energy of 4×10^{20} J is converted by a net mass loss of 4×10^{3} kg, according to the Einstein relation ($E = mc^2$). This solar radiation energy is emitted in a form as electromagnetic radiation. [23] In free outer space, The intensity of solar radiation at the average distance from the sun to the earth is 1,353 W/m^2. [23] The atmosphere attenuates the solar radiation energy when it reaches the earth. The angle degree to which the atmosphere affects the solar radiation energy received at the surface of earth is quantified by "air mass". The secant of the angle between the sun and the zenith is defined as the air mass (AM) number, which measures the atmospheric path length relative to the minimum path length when the sunlight is incident perpendicularly overhead. Hence the AM 0 represents the solar spectrum from outer space outside the earth's atmosphere. The AM1 represents the sunlight at the earth's surface when the sun is at zenith, and the incident power of AM1 is about 925 W/m^2. [23] Sunlight radiation angles and solar spectrums at various AM condition, are shown in figure 11 and figure 12 as below.

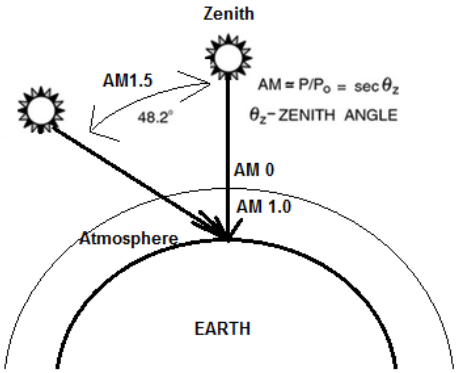

Figure 11 Sunlight radiation angles

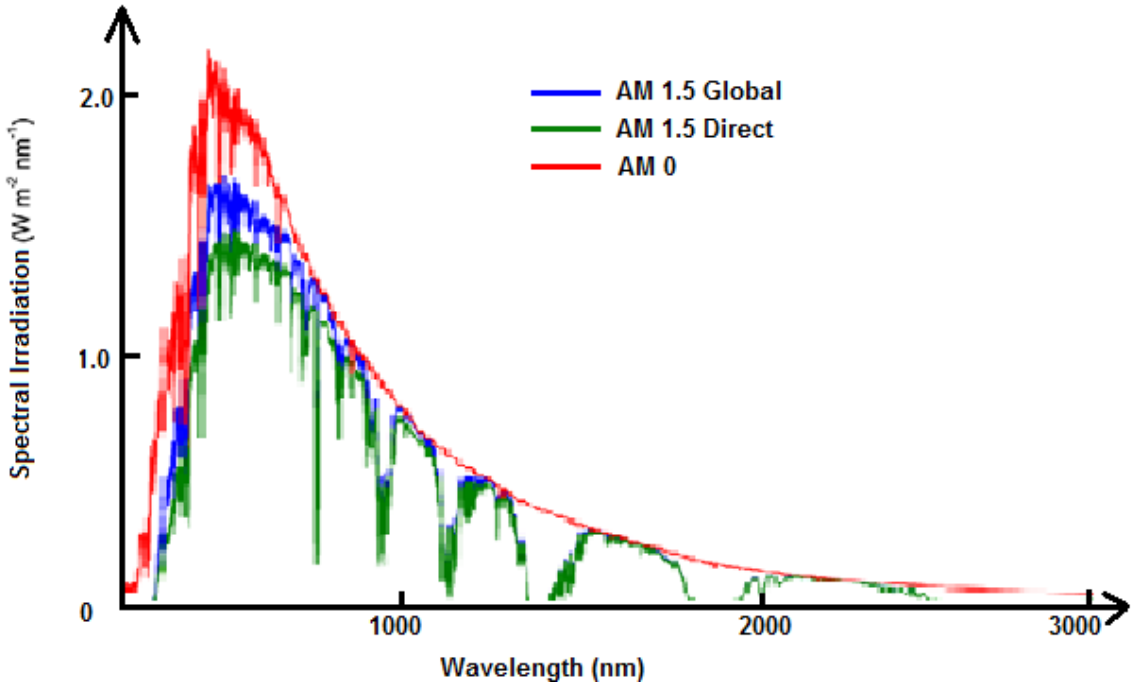

Figure 12 The solar spectrums at various AM conditions

The upper red color curve is the AM0 condition, and it can be approximated by a 5,800 K black-body radiation. The AM1.5 condition represents a satisfactory energy-weighted average for terrestrial applications. The total incident power for AM 1.5 is 844 W/m^2. [23] For solar-cell energy conversion, the solar power can be converted to photon flux, and each photon produces an electron-hole pair charge carrier.

2.5.2 Operation Theory of Solar Cell

A solar cell is also a P-N junction semiconductor device. When solar cells are exposed to incident solar radiation, only photons that have energy equal or greater than E_g can contribute energy Eg to the device output, the extra energy is transferred into heat. Photons with energy less than the band-gap Eg cannot be absorbed in a semiconductor. When the electron-hole pairs are created in the depletion layer, they are separated by the built-in electric field and flow through

the external load. [24] Energy band diagram of a P-N junction solar cell under solar irradiation is shown in figure 13 as below.

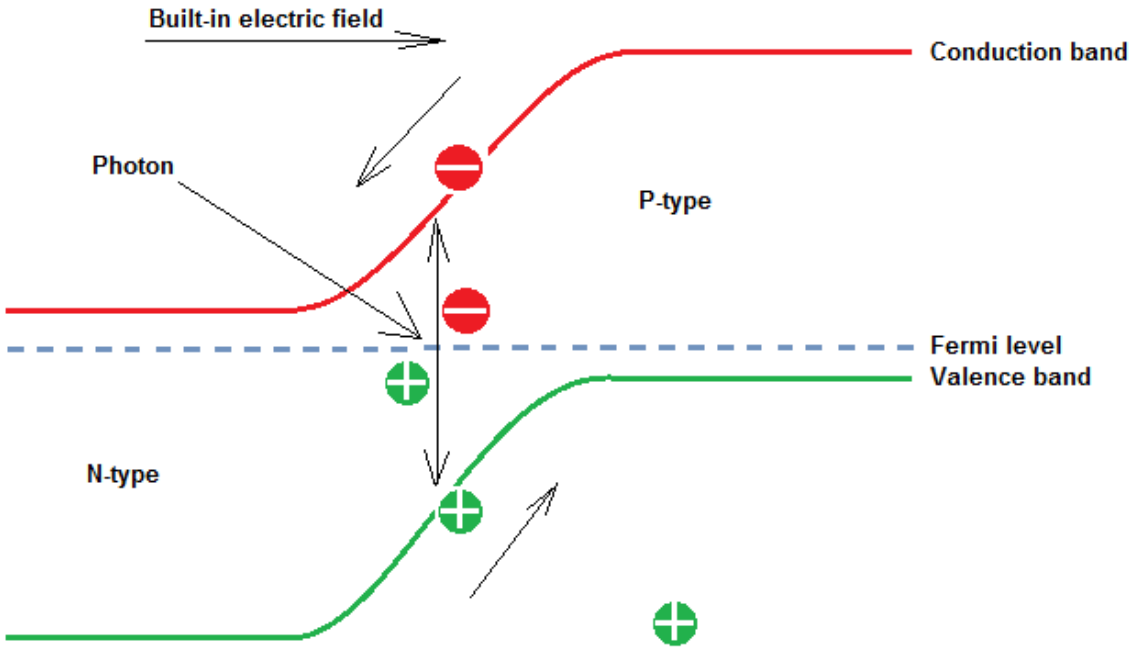

Figure 13 Energy band diagram of P-N junction solar cell with solar irradiation

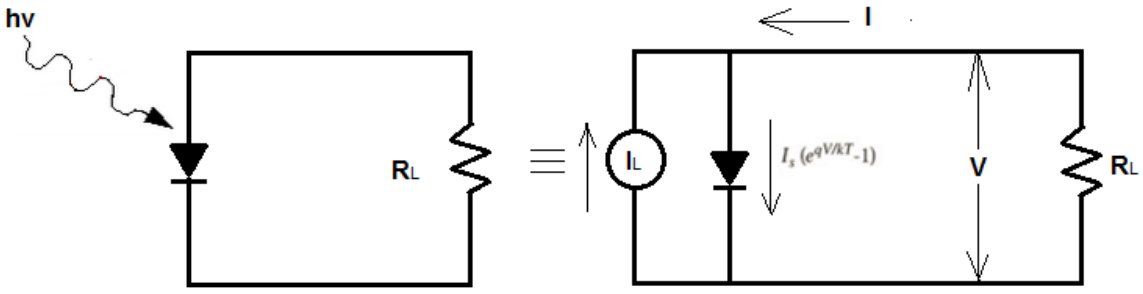

Figure 14 Idealized equivalent circuit of solar cell device

Solar cell can be assumed with ideal diode I-V characteristics. The equivalent circuit is as shown in figure 14. A constant current source I_L of photocurrent, powered by the excitation of excess carriers by solar radiation, is in parallel with the junction. I_S is the diode saturation current, and R_L is the load resistance. [24] The total I-V characteristic of solar cell device under illumination is a summation of the dark current and the photocurrent:

$$I = I_S \left(e^{qV/kT} - 1\right) - I_L$$

The open-circuit voltage, V_{OC}, is the maximum voltage available across a solar cell device, and it occurs at zero current. The open-circuit voltage equals to the amount of forward bias on the solar cell device due to the bias of the solar cell P-N junction with the light generated current. [24] The open-circuit voltage is shown on the IV curve below in figure 20. When I is equal to 0, we obtain the open-circuit voltage:

$$V_{OC} = \frac{kT}{q} \ln\left(I_L/I_s + 1\right)$$

The short-circuit current is the current through the solar cell device when the voltage across the solar cell device is zero, as the solar cell is short circuited. The short-circuit current is the largest current which may be drawn from the solar cell. [25]

The fill factor, "FF", is a parameter in conjunction with V_{oc} and I_{sc}, determines the maximum output power from solar cell device. The FF is defined as the ratio of the maximum power from the solar cell to the product of V_{oc} and I_{sc}. The FF is the area of the largest rectangle which fits in the IV curve, as the color square in figure 20 as below.

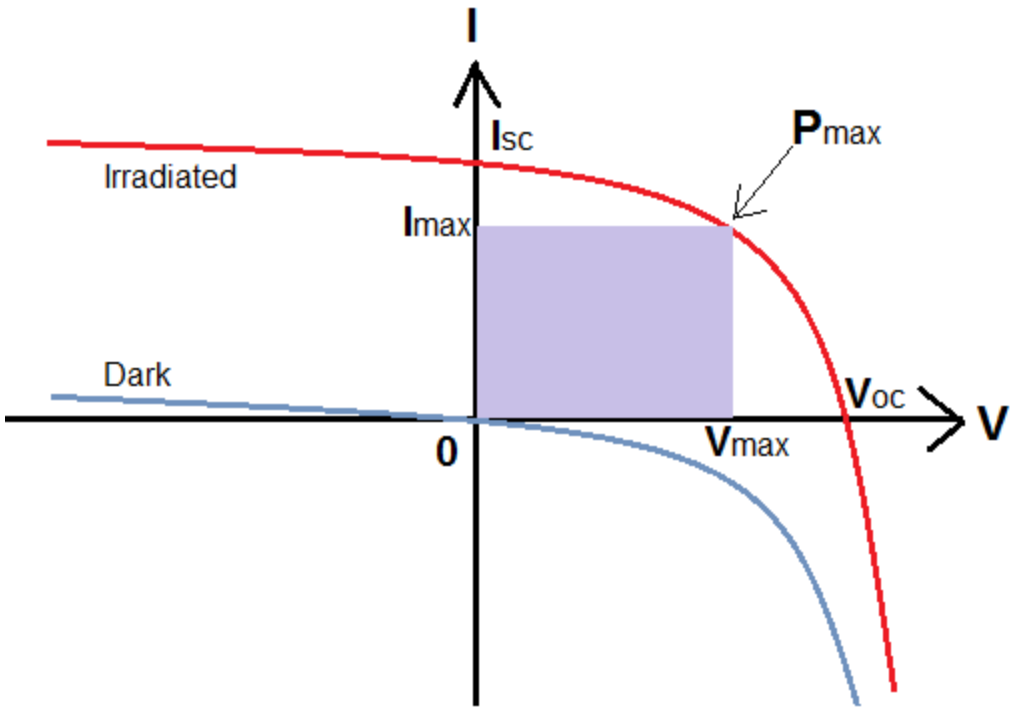

Figure 15 Fill factor at maximum current and voltage

As shown in figure 15, the FF is determined from measurement of the IV curve. And it is defined as the maximum output power divided by the product of I_{sc}*V_{oc}:

$$FF = V_{MP} I_{MP} / V_{OC} I_{SC}$$

The efficiency of a solar cell is defined as the ratio of energy output from the solar cell to input energy from solar radiation. The efficiency of a solar cell depends on, the performance of the solar cell, the spectrum and intensity of the incident sunlight and the temperature of the solar cell. Terrestrial solar cells are measured under AM1.5 conditions and at a room temperature of 25°C, and the input power for efficiency is 100 mW/cm^2. [25]

$$\eta = FF * I_{SC} * V_{OC} / P_{in}$$

Solar cell series resistance is created by the current movement through the emitter and base of solar cell device, contact resistance between metal back contact and absorber, and the resistance of top collector and back metal contacts. Series resistance reduces the fill factor, and excessively high value series resistance can also reduce the short-circuit current. Series resistance makes no effect over open-circuit voltage of a solar cell. Figure 16 is the schematic of a solar cell with series resistance. [25]

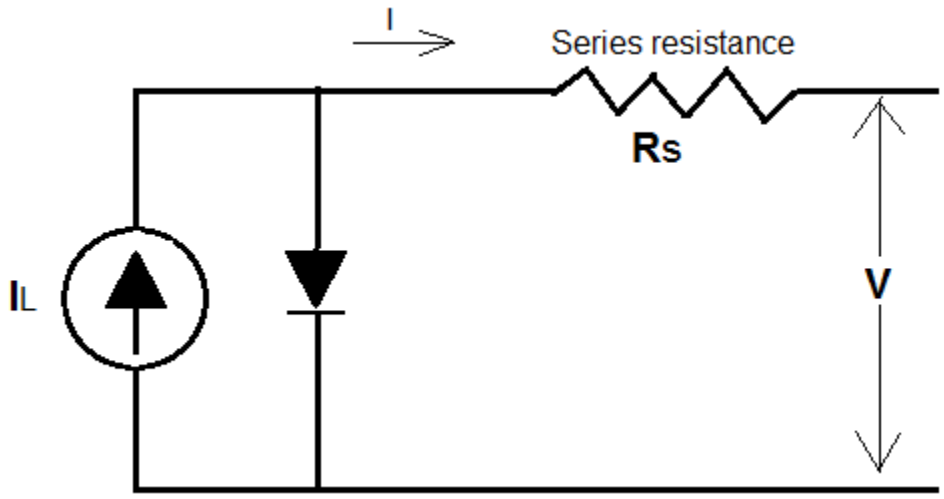

Figure 16 Schematic of a solar cell with series resistance

Shunt resistance can cause significant power losses in a solar cell. Low shunt resistance creates an alternate current path for the light-generated current, which causes power losses in solar cells. Shunt resistance causes severe effect at low light levels, due to less light-generated current. The current loss to the shunt has a greater impact on solar cell performance. Moreover, the effective resistance of solar cell is relatively high at lower voltages, so the impact of a resistance in parallel is unnegligible. Figure 17 shows a diagram of a solar cell with shunt resistance.

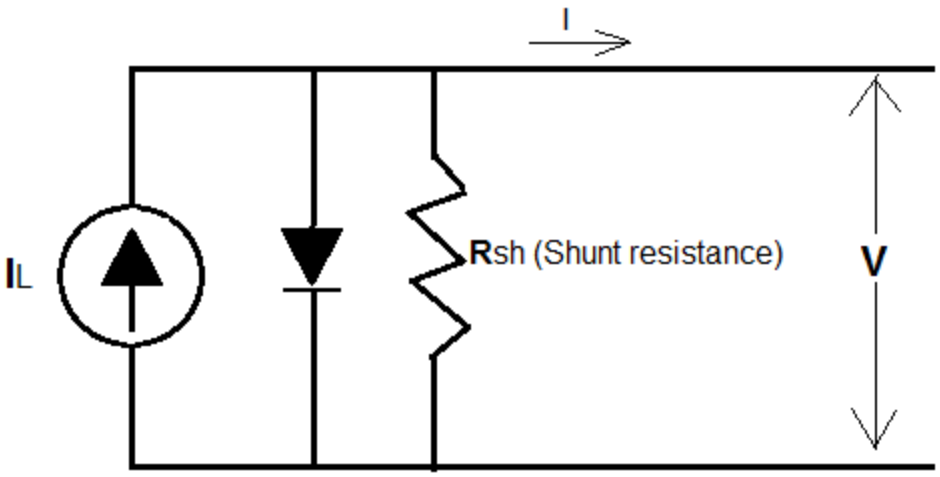

Figure 17 Circuit diagram of a solar cell including the shunt resistance

2.5.3 Thin Film Solar Cells

A thin-film solar cell is fabricated by depositing one or more thin film layers of photovoltaic semiconductor material on a substrate. The substrate could be glass, plastic or stainless steel. Thin-film solar cells are commercially used coming with several technologies, including cadmium telluride (CdTe), copper indium gallium diselenide (CIGS), and amorphous thin-film silicon (a-Si). CdTe and CIGS are all p-type semiconductors. The thickness of thin-film varies from a few nanometers to tens of micrometers, which allows thin-film solar cells to be flexible and low-weight. Thin-film solar cell is a great fit for building integrated photovoltaic applications, because they can be easily laminated onto windows. [26]

The conventional c-Si technology has the advantage over thin-film solar cell technology on efficiency performance. However, the thin-film industry has significantly improved over the past decade, and laboratory CdTe and CIGS solar cell efficiencies are now beyond 21 percent, which outperforms multi-crystalline silicon. The lifetime of thin-film solar panels are expected to be 20 years or so. To reduce the photovoltaic electricity production cost, solar cells industry needs to

optimize production processing, and consume less raw materials. Thin-film solar cells expend much less materials, compared to crystalline silicon solar cells. Also the serial connection of cells into a thin-film module can be done during the fabrication of cells. Moreover, it is possible to adjust the band gap of some thin-film semiconductor material by varying the composition, such as CIGS and CZTSSe, in order to reach better conversion efficiency. The power conversion efficiency record in laboratory scale CIGS devices has reached 21.7%. [28] Another advantage of thin-film semiconductor materials is much more tolerant of defects and grain boundaries, compared to Silicon counterparts. The only potential shortcoming of promising CIS, CIGS, and CdTe is the fact that they contain expensive and rare materials. The cost of Indium and Tellurium will become a particular issue for the anticipated deployment of thin-film photovoltaic industry on terawatt scales. Co-evaporation technique produces the best efficiencies on CIGS devices, although various other techniques are available as well, such as: reactive sputtering, CVD, etc. [27]

There are also other thin-film materials, which are still in an early stage of ongoing research and development, with limited commercial availability, including organic, dye-sensitized, and polymer solar cells, as well as quantum dot, copper zinc tin sulfide/selenide, nanocrystal, micromorph and perovskite solar cells.

2.5.4 CIGS Thin Film Solar Cell

Copper indium gallium selenide (CIGS), is an I-III-VI2 thin film semiconductor material composed of copper, indium, gallium, and selenium. The material is a solid solution of copper indium selenide and copper gallium selenide. It has a chemical formula of $CuIn_xGa_{(1-x)}Se_2$, where the value of x can vary from 1 (pure copper indium selenide) to 0 (pure copper gallium

selenide). CIGS has a chalcopyrite crystal structure, and a band-gap varying continuously with x from about 1.0 eV (for copper indium selenide) to about 1.7 eV (for copper gallium selenide). CIGS is also a tetrahedrally bonded semiconductor. [27] In spite of the difference of the various thin-film compound materials, most thin-film solar cells share a similar device structure. Figure 23 shows the structure of CIGS thin-film solar cell. For CIGS, the most suitable back contact has been proven to be Molybdenum. The thickness is 0.5-1 micrometer and the molybdenum is commonly sputtered on the glass. CIGS absorber is deposited on top of Molybdenum back contact. The main electron-hole pair production takes place in the CIGS absorber. Figure 18 shows the cross section of a typical CIGS solar cell.

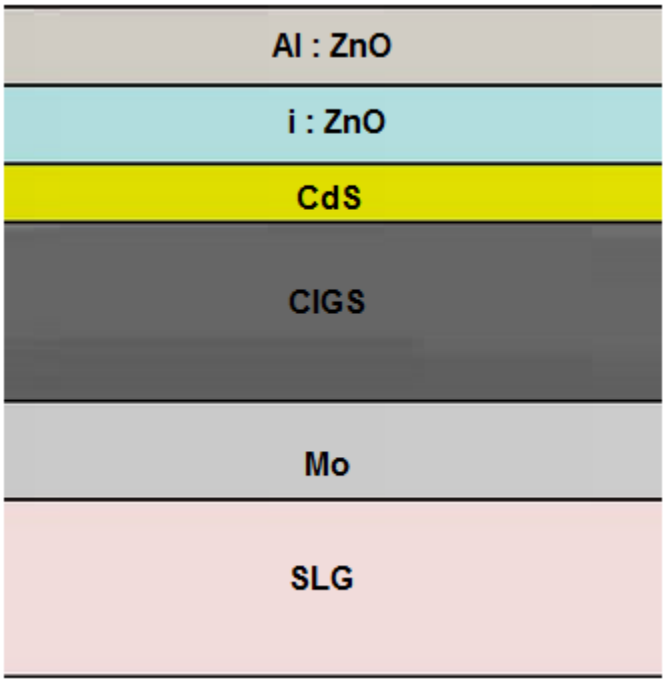

Figure 18 Cross section of a typical CIGS solar cell

The CIGS absorber has a thickness of around 2–4µm. A chemical bath deposition (CBD) process is followed to produce a buffer layer of Cadmium Sulfide, which improves the lattice matching

between absorber and ZnO layer. An layer of intrinsic zinc oxide (i-ZnO) is overlaid on top of CdS, before the deposition of the transparent conducting oxide window layer, Al doped ZnO (ZnO:Al), which provides the needed conductivity. Furthermore, an anti-reflection coating is introduced too optionally, to increase incoming light.

2.5.5 CZTS Thin Film Solar Cell Family

Copper zinc tin sulfide (CZTS) is a quaternary semiconductor material which has received increasing attention in solar cell application. Its related materials include other I_2-II-IV-VI_4 such as copper zinc tin selenide (CZTSe) and the sulfur-selenium alloy CZTSSe. CZTS offers favorable optical and electronic properties similar to CIGS (copper indium gallium selenide), and that makes it well suited to be used as a thin-film solar cell absorber layer. But unlike CIGS, or other thin films such as CdTe, CZTS is only composed of abundant and non-toxic elements. Concerns with the cost and availability of indium in CIGS and tellurium in CdTe, plus the toxicity of cadmium have been large motivators in searching for alternative thin film solar cell materials, such as CZTS. Recent CZTS material improvements have enabled the efficiency of CZTS thin film solar cell to increase to 12.6% in laboratory scale, but there is still a lot of work before the potential commercialization of CZTS thin film solar cells.

$Cu_2ZnSnSe_4$ and Cu_2ZnSnS_4 are notionally derived from $CuInS_2$ by substituting two Indium atoms with Zn and Sn atoms. Indium is relatively rare and expensive, so people are trying to replace Indium with earth abundant and cheaper elements Zinc and Tin. Zinc and Tin are respectively produced in quantity 20,000 and 500 times bigger than Indium. [2] Also the quaternary Cu-Zn-Sn-S/Se system has a Kesterite structure, which provides additional rooms for material optimization by controlling the compositions. [29] CZTSSe is a p-type semiconductor

compound family, and the band gap of CZTSSe ranges between 1.0-1.5 eV, which is the optimum band gap for conversion efficiency. Absorbance measurements are not suitable for giving the band-gap of CZTS, because of defect absorption and the existence of secondary phases, such as ZnSe and CuSnSe. Photoluminescence measurements confirm that the band-gap of $Cu_2ZnSnSe_4$ is about 0.9-1.0 eV at room temperature. [29] The absorption coefficient, 10^4 cm^{-1}, is also suitable for thin-film application. Recently the conversion efficiency of CZTSSe has reach a new record of 12.6%. And pure sulfide Cu_2ZnSnS_4 has reached an efficiency of 8.4%, while pure selenide $Cu_2ZnSnSe_4$ has arrived an efficiency of 9.15%. [10] The crystal structure of CZTSSe has been reported experimentally to have two options: Kesterite and Stannite. [30] These two crystal structures are very similar, in both structures the metals are located on the tetrahedral sites, but their distributions on planes perpendicular to the c-axis are not the identical, and the location of the chalcogen is slightly different. From the calculation of first-principles theoretical method within DFT (density functional theory), the lattice constants of CZTS structures are given in Table 1. Total energy calculation shows kesterite structure is better than stannite on stability. [29]

Table 1 Lattice constant of Kesterite and Stannite of CZTSe and CZTS

Lattice constant	$Cu_2ZnSnSe_4$		Cu_2ZnSnS_4	
	Kesterite	Stannite	Kesterite	Stannite
a (nm)	0.5732	0.5738	0.5441	0.5455
c (nm)	1.1418	1.1453	1.0864	1.0878

CZTS, as a photovoltaic semiconductor material, is first reported by K. Ito and T. Nakazawa in 1988, a photovoltaic effect is recorded at a junction of CZTS and $CdSnO_2$. [31] Great

improvements have been done on conversion efficiency since 2000. Hironori Katagiri's team has reached 6.7% efficiency by using preferential etching technique in 2007. [32] By using solution based nanocrystals method to deposit precursors followed by heating with Sulfur, an efficiency of 7.2% has been accomplished in 2011. [33] IBM made a new record of 10.2% on CZTSSe in 2012, and recently they just improve it to 12.6%. [34] Despite this promising progress, most works have been done on fabrication of devices, theoretical understanding of the material is still very limited. The fabrication processes of CZTS can be defined in two categories, "One-stage" and "Two-stage" techniques.

Unlike the CIGS material, the best devices of CZTS have always been produced by a two-stage method, and two-stage methods are the most popular approaches at present. The first stage is to prepare the precursors, normally at room temperature. The precursors could be only metal precursors or all elements including Sulphur or/and Selenium. The first stage can be processed in various ways, such as Thermal Evaporation, Electron Beam Evaporation, Sputtering, Pulsed Laser Deposition, Spray Pyrolysis, Electrodeposition, and Nanopaiticle Printing. [35] The reaction process normally happens in the second stage, while the substrates are heated, in an atmosphere containing sources of Sulphur or/and Selenium, this stage is normally referred as "sulfurisation" and "selenization". The purpose of this stage is to form crystallization of the desired phases from precursors. And it is this stage of crystallization makes the most influential effect on the device performance. A typical approach is to heat substrates to 500-600 ℃ in a H_2S and N_2 environment for 2-4 hours. [36] Recently the best devices went through multi-steps of deposition and selenization processes. Other deposition techniques include: hybrid solution-particle technique, electrodeposition, co-evaporation, sputtering, OA-CVD (Open Atmosphere Chemical Vapor Deposition), nanoparticles, and sol-gel.

One-stage method fabricates CZTS thin-film in a single step, where all the elements are incorporated simultaneously, such as co-evaporation of all elements with substrate heated. The selenization process is ongoing with the co-evaporation of elements, this method is adopted from CIGS fabrication experience. More results from the solar industry are shown in figure 19.

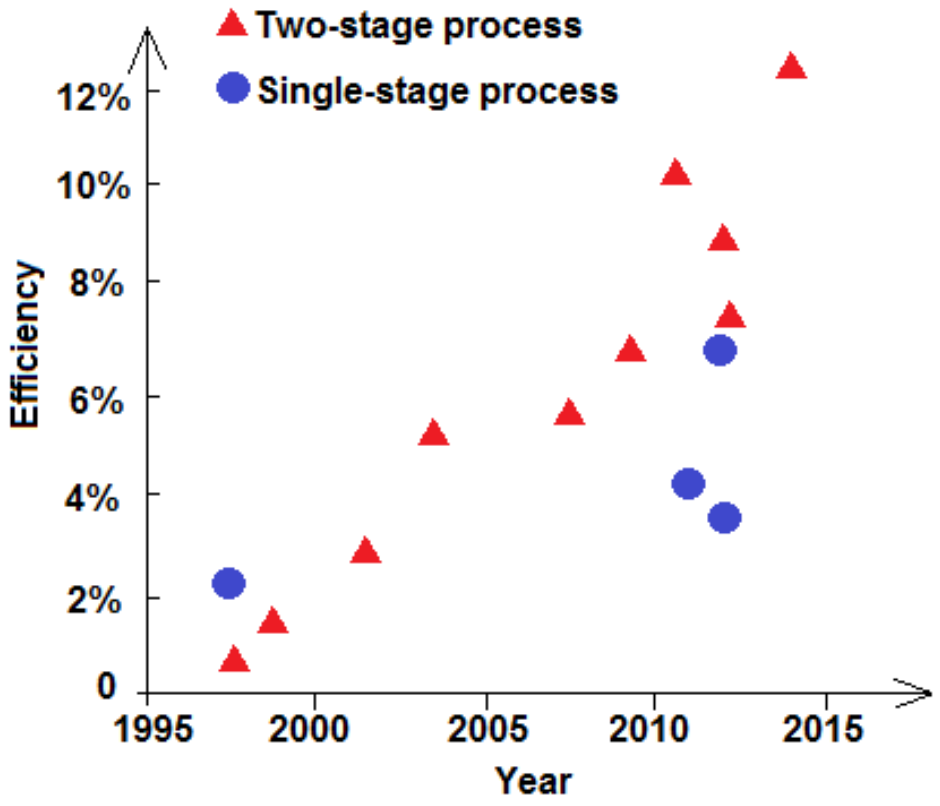

Figure 19 CZTS thin-film devices performance comparison on “One-stage” process and “Two-stage” process

CHAPTER 3: DEVICE FABRICATION AND CHARACTERIZATION TECHNOLOGIES

3.1 Device Structure

Figure 25 shows the device structure of a Mo/CZTSe/CdS/ZnO solar cell. The multiple layers of the device are fabricated by a sequential deposition procedure.

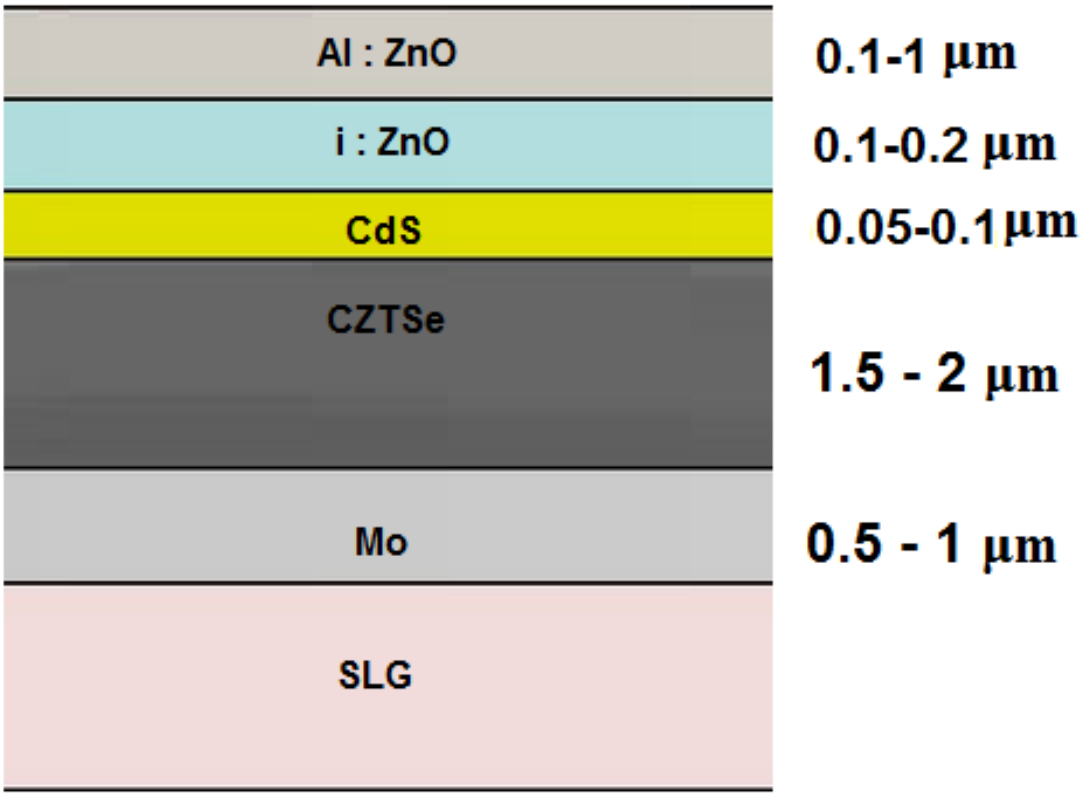

Figure 20 Device structure of a CZTSe/CdS/ZnO solar cell

As shown in figure 20, the device structure is a piece of 2-millimeter thick soda-lime glass. The sodium contained soda-lime glass has been proven helpful to create a greater open-circuit voltage in CIGS research, suggesting sodium acts through passivation of grain-boundary defects. [37] A molybdenum (Mo) metal layer is deposited (by DC sputtering), and it serves as the back contact, while it also reflects unabsorbed light back into the absorber. On top of molybdenum layer, a p-type CZTSe absorber layer is grown by two-stage process. A thin n-type cadmium sulfide (CdS) buffer layer is added on top of the absorber. This CdS buffer layer is deposited via a chemical bath deposition process. The buffer layer is followed by a thin intrinsic zinc oxide layer (i-ZnO). The front contact layer is a thicker aluminum (Al) doped ZnO layer. Both i-ZnO layer and Al:ZnO layer are deposited by RF sputtering. The thin i-ZnO layer is used to protect the CdS layer and the absorber layer from potential sputtering damage during the Al:ZnO deposition. [38] The Al doped ZnO layer serves as the front contact. It is transparent conducting oxide, and it collects and conducts electrons out of the device, while absorbs little input light, so most of incident light could reach the CZTSe absorber.

3.1.1 Substrate

As for CIGS thin-film solar cells, soda-lime glass substrates are popularly used for CZTSe thin-film solar cell fabrication, due to the low costs, corrosion resistance, and sodium content. Sodium incorporation from soda-lime glass into the CZTSe absorber has been reported as an advantage to improve the performance of CZTSe solar cell devices. [39] Sodium incorporation into CZTSe substantially improves the device efficiency by enhancing the open-circuit voltage and fill factor. During the high temperature selenization process, the sodium atoms diffuse into the bulk of CZTSe absorber. And sodium diffusion in CZTSe absorber was found to affect grain size, crystal texture, and conductivity. [40] Sodium is reported as helping increasing hole density, making the

acceptor shallower, shifting the Fermi level lower, and leading to higher built-in voltage and higher open-circuit voltage. Sodium also reduces the concentration of recombination centers, and this also improves open-circuit voltage. The increase of hole density and mobility improves the fill factor by enhancing CZTSe absorber conductivity. [39] Ordinary store bought soda lime glass has been used in this research. Preheating Molybdenum coated glass substrates have been done in order to enhance the sodium diffusion in the CZTSe absorbers.

3.1.2 Back Contact

Molybdenum has been used as the back contact of CZTSe solar cells. There are some required properties for metallic materials as the back contact, such as, good adhesion to the soda-lime glass substrates; low self resistivity; formation of ohmic contact with the CZTSe absorbers; high resistance to selenium corrosion; appropriate thermal expansion coefficients matched to both the soda lime glass substrates and to CZTSe absorbers; chemical inertness with Cu, Zn and Sn; high stability during the subsequent fabrication process; and function as a proper transportation medium for sodium diffusion from soda lime glass substrate into CZTSe absorber. Molybdenum has been proven as the best back contact choice of our CZTSe solar cell fabrication. [40]

DC magnetron sputtering has been used to deposit molybdenum onto the soda lime glass substrate. The DC sputtering process condition parameters determine the quality of the molybdenum layer. The working pressure has a significant impact on the properties of molybdenum films by determining the resistivity and adhesion of the molybdenum layer to soda lime glass. Lower working pressure produces molybdenum layer with higher density, lower resistivity, and smoother surface. However, molybdenum layer produced at lower working pressure also suffers poor adhesion problems to the soda lime glass, because of compressive

stresses. Also high sputtering power and low sputtering voltage reduces the resistivity and enhances the adhesion of molybdenum film. In order to achieve good electrical properties and good adhesion to soda lime glass substrate, a bi-layer deposition process has been used. The deposition starts at a higher working pressure (10 mTorr) for the first 100nm thickness of molybdenum layer, and then it is reduced generally to a lower level (2-3 mTorr). The rest of deposition is finished at the fixed lower working pressure(2-3 mTorr). During the selenization process of CZTSe absorber, an intermediate $MoSe_2$ layer would be produced, and it forms a quasi-ohmic transport contact system at the interface of CZTSe layer and molybdenum layer. If this $MoSe_2$ is thin enough, it might not affect device performance too much, however if the $MoSe_2$ is too thick, it deteriorates the performance of CZTSe thin-film solar cell devices, and even causes CZTSe films peeling off from substrates.

Molybdenum films are deposited by DC magnetron sputtering on soda-lime glass substrates. The molybdenum target in use is a size of 3 inches in diameter with a purity of 99.95%. Before deposition, the soda-lime glass substrates (25mm × 20mm × 5mm) are ultrasonically cleaned in acetone, methanol and deionized water sequentially for 30 min, and subsequently blow-dried with nitrogen gas. The soda-lime glass substrates are loaded onto a substrate holder, then pushed into the sputtering system chamber. And the distance between target and substrate is 10 cm. The chamber is evacuated to a base pressure of 1.5×10^{-6} Torr. The substrate is heated for 10 minutes before Molybdenum deposition to remove moisture. The substrate temperature increases during the depositing due to the bombardments of the sputtering particles, and the final temperature of substrate is about 80℃. The Ar (99.999+%) gas flow rate is adjusted to 75 sccm at the beginning, then decreased to 8 sccm gradually, to create a thin but better adhesion layer of molybdenum on substrate at the beginning. To obtain the better surface homogeneity of

molybdenum layers, the substrates are rotated by a motor during deposition. The effects of deposition parameters include working pressure, sputtering power and sputtering voltage. The deposition parameters and the corresponding ranges for molybdenum film depositions are listed in table 2. For the molybdenum layers with a bi-layer structure, a thinner layer is deposited under the higher working pressure, which is followed by the deposition of the second molybdenum layer under lower working pressure. [40] The total thickness of molybdenum layers is 0.5-1μm. The electrical resistivity of molybdenum layers is measured by the four-point probe technique. The lowest sheet resistance of 100nm thick molybdenum film is 0.8Ω/sq.

Table 2 Deposition parameters for DC magnetron sputtering molybdenum layers

Deposition parameter	**Layer 1**	**Layer 2**
Working pressure	10mTorr	2 mTorr
DC sputtering power	100w	300 W
Sputtering voltage	280 V	450 V
Thickness	100nm	500nm to 900 nm

3.1.3 Cadmium Sulfide

The Cadmium Sulfide layer in CZTSe solar cell is a thin buffer layer is added on top of the absorber. Since it is n-type, it enables the formation of a p-n junction with p-type CZTSe. Cadmium sulfide layer also protects the absorber from damage caused by the subsequent RF in:ZnO deposition. CdS crystallizes in different structures, and the most common form is the hexagonal wurtzite structure. The two other lattice forms are the face-centred zincblende-structure and the high-pressure NaCl phase. [41] CdS is a direct band-gap semiconductor, and its band-gap is 2.42eV. CdS is mostly transparent in the lower and visible part of the solar spectrum,

allowing the solar light to penetrate into the CZTSe absorber layer thus giving rise to the photovoltaic effect. CdS absorbs high energy photons of the visible spectrum, with an absorption rage shorter than 505nm.

Poor properties of the CdS layer causes low hole lifetime and high recombination. Photo-generated carriers in CdS layer contribute negligible photocurrent, therefore constitutes a current loss at lower wavelength range. To minimize these losses, it is necessary to minimize the thickness of the CdS layer. However if the thickness of CdS layer is too thin, it also deteriorates the P-N junction quality in the solar cell device, due to possible formation of pinholes which will create parallel junctions. [41]

Although cadmium sulfide deposition can be done by multiply methods, such as chemical bath deposition, closed spaced sublimation (CSS) and RF sputtering. Chemical bath deposition (CBD) is the most popular deposition method, because of its low cost, simple facility setup and better performance of uniformity of CdS thin-film. CdS buffer layer increases excess carrier lifetime, and it optimizes the band alignment of the device, also that it provides an improved lattice matching at the heterojunction interface. [41]

Chemical bath deposition requires simple setup, only solution beakers and sample mounting devices. The drawback of chemical bath deposition is the wastage of solution. Chemical bath deposition produces stable, adherent, uniform and great quality thin-films. The growth of thin films strongly depends on growth conditions, such as duration of deposition, solution composition and temperature of the solution, and topographical and chemical nature of the substrate. The solutions used for chemical bath deposition of cadmium sulfide are cadmium acetate (cadmium source), thiourea (sulfur source), and ammonium hydroxide (complexing

agent). Solar cell device performance is found to be dependent on the CdS layer thickness, but rather independent on the reaction temperature. [41] A thickness of 60-80nm CdS layer is preferred, to get the best results for Voc and fill factor.

A thin layer of CdS, about 50nm, is deposited on the CZTSe absorber by chemical bath deposition method. The solution is composed of 406 ml of DI water, 99 ml of NH_4OH ammonium hydroxide (20-22%), 60 ml of cadmium acetate (0.015M/L $CdSO_4$), and 60 ml of thiourea (0.15M/L NH_2CSNH_2).

Table 3 Solutions parameters used in CBD process

Solutions	Concentration	Volume
DI water	NA	406 ml
NH_4OH ammonium hydroxide	20-22% w/w	99ml
Cadmium Acetate	0.015M/L	60ml
Thiourea	0. 15M/L	60ml

The bath solution is contained in a well cleaned one liter beaker, in which is constantly stirred by a magnetic stirrer through the deposition process. The solution components are mixed in the beaker at room temperature. The solution is headed up to 75 ℃, and stay there for 9-10 minutes. The nucleation starts at approximately 6 minute, and then coalescence and continuous growth on sample are attained after 9-10 minutes deposition. The reactions for formation of the CdS thin-film can be written as below:

$$NH_3 + H_2O \rightarrow NH^{4+} + OH^-$$

$$Cd^{2+} + 4NH_3 \rightarrow Cd(NH3)_4^{2+}$$

$$(NH_2)_2CS + OH^- \rightarrow CH_2N_2 + H_2O + HS^-$$

$$HS^- + OH^- \rightarrow S^{2-} + H_2O$$

$$Cd(NH_3)_4^{2+} + S^{2-} \rightarrow CdS + 4NH_3$$

3.1.4 CZTSe Thin Film Absorber Fabrication

CZTSe thin-film absorbers have been fabricated by a two-step rapid thermal process. Depositions stacks of metallic precursors are followed by selenization in a selenium vapor atmosphere for two annealing temperature stages. Compared to popular co-evaporation process, this two-step rapid thermal process is more feasible to commercial mass production. Because this two-step process separates metallic depositions and selenization into sequential processes from individual elemental sources, this technique is more controllable, compared to co-evaporation technique. And by using this two-step technique, high compositional uniformity of large scale depositions and coatings can be easier obtained than one-step co-evaporation process.

Copper, Tin, and Zinc metallic precursor stacks have been deposited in a special designed order onto Molybdenum coated soda-lime glass substrates. The metallic stack order is selected to minimize tin loss during the selenization process. Due to the complexity of this quaternary compound system, compositional parameters play a crucial role on the properties of CZTSe thin-films. The metallic precursor depositions have been operated in zinc-rich and copper-poor conditions, since there is a general conclusion that zinc-rich and copper-poor conditions are beneficial for the properties of CZTSe kesterite system. Zinc-rich and copper-poor conditions help to avoid the formation of the ternary compound Cu_2SnSe_3, which is known to reduce the

open circuit voltage. The zinc concentration needs to be high enough to prevent the formation of Cu_2SnSe_3, but as low as possible to minimize the formation of secondary phase ZnSe. [42]

The CZTSe thin-film has been fabricated in a two-station vacuum chamber. The metallic precursors have been deposited in the first chamber station at a base pressure of 5×10^{-6} Torr. Copper, Zinc, and Tin are deposited separately through thermal evaporation from three metallic thermal effusion cell evaporators. Radak evaporator effusion cells allow a great control of source temperature and avoid spitting of the sources. Alumina crucibles are equipped inside the evaporator effusion cells. Pneumatic substrate shutters are attached above the thermal evaporator effusion cells to minimize cross contamination. Pneumatic shutters are also placed underneath the sample holder to isolate the substrate from the source during the source stabilization. Shields are placed to separate effusion cells. The purities of copper, zinc, and tin pellets are 99.999%. Quartz crystals have been used to monitor the metallic precursor deposition thickness. The two-station chamber itself is double jacketed and water cooled.

Figure 21 shows the two-station vacuum chamber that has been used for CZTSe thin-film fabrication. Molybdenum coated substrates are fastened on a sample holder, and then loaded into the load-lock on the left side of the chamber system. A magnetically coupled arm is used to transport the sample through stations. The two-station chamber is equipped with linear drive motors connected with a prong and a thermocouple in each station. The prongs grab and hold the sample holder during the deposition processes. Turbo pumps are used for both chamber stations to achieve a base working pressure of 5×10^{-6} Torr. Dedicated quartz crystal monitors are used to monitor the thickness of depositions. The deposition temperatures for metal precursor depositions are shown in table 4 in below.

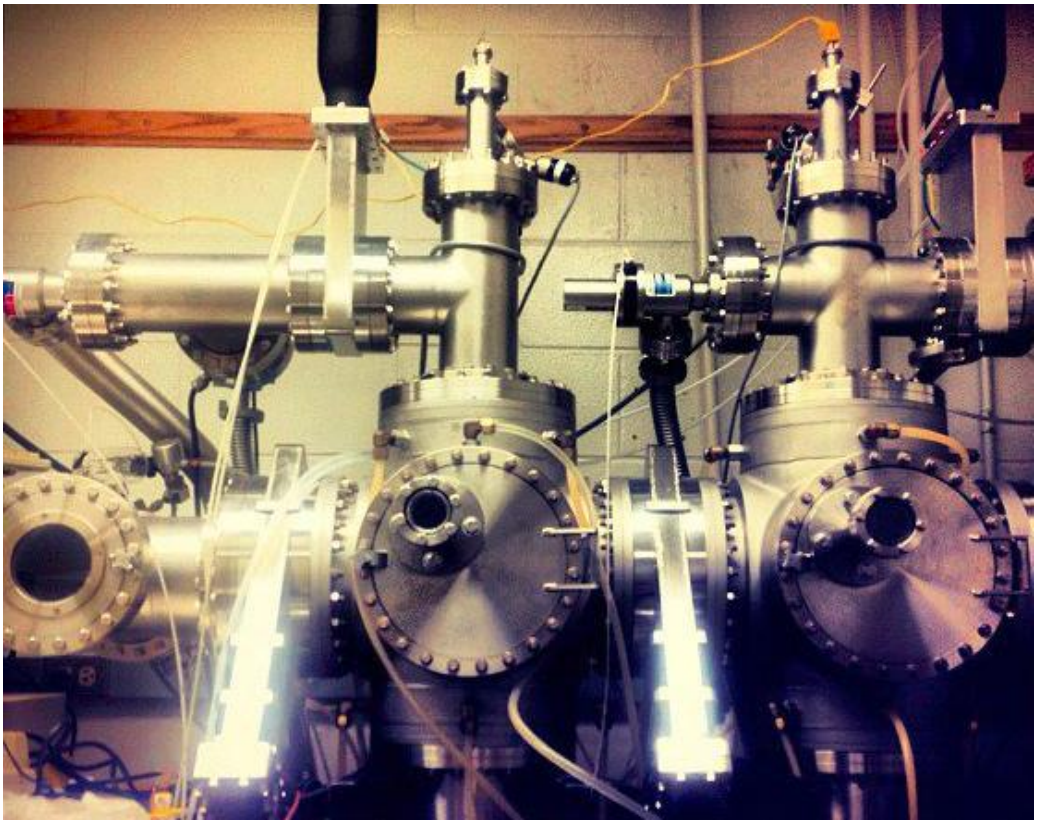

Figure 21 Metallic precursor deposition and selenization chamber

Table 4 Deposition temperatures for metal precursors depositions

Metal precursors	Effusion cell temperature
Cu	1185 ℃
Zn	350 ℃
Sn	1200 ℃

The selenization process is carried out in the second station of chamber. The substrate is heated up by using a Sylvania/Osram FHM (1000W/120V) lamp. Various selenization processes have

been tried out at different substrate temperatures from 320-550℃, with and without additional tin supplement. The selenium effusion cell temperatures have been carried out from 210℃ to 245℃, in order to produce a range of different selenium vapor fluxes, from 5-15 Å/s. The working pressure is about 9 x 10^{-5} Torr.

3.1.5 Intrinsic ZnO Layer Deposition

Zinc oxide is an n-type semiconductor material with a hexagonal crystal structure of wurtzite, a wide and direct band gap of 3.37 eV at room temperature, and a high exaction binding energy of 60 meV. Undoped ZnO thin film material normally exhibits n-type conductivity with a background electron concentration very high. [43] The electrical conductivity of undoped ZnO is due to intrinsic defects, such as oxygen vacancies and interstitial zinc atoms. ZnO has been proven to be the most promising transparent conducting oxides material for CZTSe thin-film solar cells, due to its properties of high conductivity, good transparency and lower cost. Sputtering deposition of ZnO films has been known as a damage process to the underlying CdS layer, also produce dislocations and defects at the interface. This is caused by the collisions of high energetic particles from target. In order to limit the disadvantages of sputtering on device performance, bi-layer ZnO films have been applied, in which the intrinsic undoped i-ZnO layer is deposited before the low-resistive n-type Al:ZnO layer. This inserted thin intrinsic undoped ZnO layer helps to improve cell performance. Because it helps to avoid a degradation of the interface on CdS layer, from penetration of aluminum from ZnO:Al layer and the damage of CdS layer from sputtering particles. It also functions as a seed layer which enhances the grain growth of the subsequent n-type Al:ZnO layer. [43] Many growth techniques such as RF magnetron sputtering, spray pyrolysis, metalorganic chemical vapor deposition, pulsed laser deposition, have been used to fabricate ZnO layer. The most commonly used technique is sputtering,

because it avoids using toxic gases, reduces losses and produces good thin film uniformity with desired crystallographic orientation even at lower substrate temperature. RF magnetron sputtering is the least damaging growth technique. It generates relatively low energy particles and uses high plasma density and high ion/neutral ratio, therefore much lower power is required. Intrinsic ZnO thin-film is deposited in an argon/oxygen ambient with 10% oxygen, which could oxidize the intrinsic defects such as interstitial zinc atoms and occupy oxygen vacancies within the undoped ZnO film. In this research, 50nm to 100nm thickness of intrinsic ZnO is deposited on top of CdS layer. The properties of sputtered ZnO thin films depend on RF power, working pressure, thermal annealing temperature, and ambient atmosphere.

The i:ZnO is deposited by using a RF magnetron sputtering system at room temperature. The RF magnetron sputtering system consists of a load lock chamber and a main process chamber, where the undoped ZnO target and Al:ZnO target are located. This system enables the insertion of sample holder into the main process chamber through a load locked chamber without breaking vacuum. Three-inch diameter ZnO and ZnO:Al_2O_3 2 wt% (99.99%) targets are employed to make intrinsic undoped and Al-doped ZnO layers. The n-type ZnO layer is deposited in pure argon ambient. [43] The i-ZnO is deposited in a pure argon and oxygen mixture ambient with 10% oxygen. It has been reported that the oxygen incorporation substantially reduces the optical absorption loss of the subsequently deposited Al:ZnO layer, improves the electronic properties of the underlying CZTSe film by increasing carrier density, lowering defect level, and increasing diffusion length, eventually enhancing Isc, Voc, and fill factor. [43] Because it accelerates the diffusion of Na towards the CdS/CZTSe junction, eventually results in the enhanced photovoltaic efficiencies. [44]

The quality of this undoped intrinsic ZnO film is controlled by the amount of the oxygen content within the gas mixture. Before deposition, a 5 minute pre-sputtering process is performed in order to remove impurities on ZnO target surface. During the deposition, the substrate holder continuously rotated by a motor to enhance film uniformity. [43] The base pressure in chamber is 1.5×10^{-6} Torr. The working pressure during the deposition is in the range from 3-5 mTorr. The Ar/O_2 (10%) gas flow rate is 12 sccm (cubic centimeters per minute at standard temperature and pressure), while the discharge power is between 160W-180W. The thickness of the ZnO thin-film layers is measured by using Dektak 3030 Surface Profiler. Sheet resistance is measured with a four probe measurement method.

3.1.6 ZnO:Al Layer Deposition

Transparent and conductive ZnO:Al layers are deposited onto intrinsic ZnO layer by using a RF magnetron sputtering system coming with a three-inch ceramic $ZnO:Al_2O_3$(2 wt.%) target. The samples are covered with a mask before the ZnO:Al deposition. The samples are heated up to 150 ℃ to gain a better conductivity of ZnO:Al layer. [45] During the deposition, the substrate holder is continuously rotated by a motor to enhance film uniformity. The base pressure in chamber is 1.5×10^{-6} Torr. The target is pre-sputtered for 3 minutes to remove the impurities on the target surface. The argon gas flow is 6 sccm, while the discharge power is around 180 W. The working pressure during the deposition is in the range from 3-5 mTorr. The total thickness of ZnO:Al layer is in a range of 200nm- 400nm. The electrical resistivity of ZnO:Al layers is measured by the four-point probe technique. The best sheet resistance we get is 90 Ω/sq.

3.2 Device Characterization Technologies

The CZTSe absorber thin-film samples are characterized by Raman spectroscopy and SEM&EDS (Scanning Electron Microscopy & Energy-dispersive X-ray spectroscopy) to measure sample composition and phases. The CZTSe thin-film devices have been characterized with current-voltage measurements and spectral response measurements to determine device performance.

3.2.1 Current-Voltage Measurement

The performance of CZTSe thin-film solar cell devices, such as Voc, Isc and FF, can be acquired by the current-voltage measurement. The current-voltage measurement is done by performing an IV sweep, which is to scan an applied voltage across the solar cell and measure the current response of the solar cell. A solar simulator system, a calibrated light source, a Keithley 2410 sourcemeter, and a labview program are used. The Keithley 2410 sourcemeter is connected to a desktop computer, which runs a labview program. The Keithley 2410 sourcemeter generates the sweeping voltage, and measures the current flowing out of the device. A four-probe method is used, as two probes from the Keithley 2410 are placed on the front contact of the CZTSe thin-film solar cell device, while the other two probes are placed on back contact of the solar cell device. This four-probe arrangement helps to eliminate the contact resistance between the probe and contact interfaces. The intensity of input light is 100 mW/cm^2 (1 kW/m^2, one-sun of illumination), and solar cell devices are measured at room temperature, around 25 °C. The voltage is swept from -1.0 volt to +1.0 volt for the light current-voltage measurement, and -0.5 volt to 1.5 volt for the dark current-voltage measurement. The labview program plots a current voltage curve, in which the current of the solar cell is plotted on y-axis against the applied

voltage on x-axis. The labview program generates the values of Voc, Isc and FF accordingly. However, the Isc generated from I-V curve is not very accurate, and we calibrate the value of Isc in the spectral response measurement by integrating current across the spectra. Figure 22 shows a dark IV curve, a light IV curve and the information about the device they reveal.

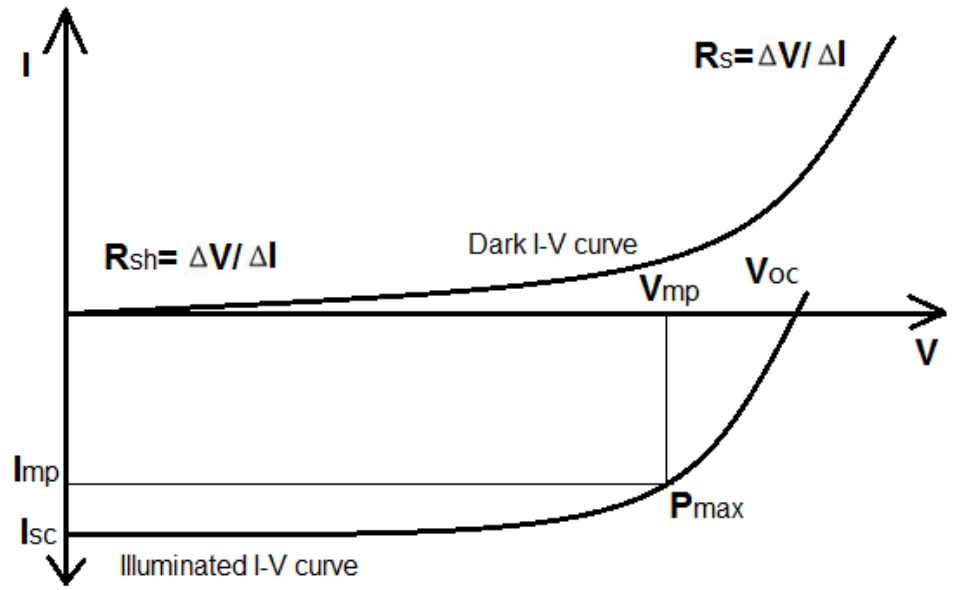

Figure 22 Dark IV curve and light IV curve above revealing information about the diode

3.2.2 Raman Spectroscopy

Raman spectroscopy is a vibrational spectroscopic characterization technique used to detect inorganic and organic materials and measure the crystallinity of solid mateials. It is sensitive to strain, so it can be used to detect stress in semiconductor materials, and it is free from charging effects. [46]

When a sample is illuminated by a laser beam, the monochromatic light from a laser interacts with molecular vibrations, phonons or other excitations in the sample material, and the energy of the laser photons is shifted up or down or called “scattered”. The shift in laser photon energy

gives information about the vibrational modes in the sample, and can be identified. The scattered light contains wavelengths that were incident on the sample and different wavelengths that represent the interaction of the incident light with the sample material. The interaction of the incident light with optical phonons is called Raman scattering. [46] The scattered light is passed through a double monochromator and the Raman-shifted wavelengths are detected by a photodetector. This technique is non-destructive and it does not require contact with the sample. Most semiconductor materials can be characterized by Raman spectroscopy. The wavelengths of the scattered light are analyzed and matched to known wavelengths for identification and composition determination. The Raman spectroscopy curves of some samples are shown in Figure 23.

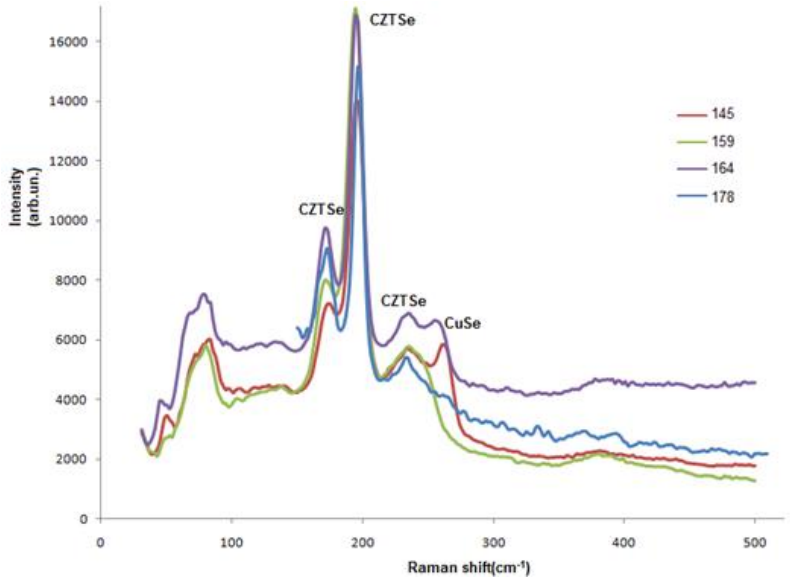

Figure 23 Raman spectroscopy of samples at different annealing temperature

Raman spectroscopy has been used to identify secondary phases in CZTSe absorbers. The Raman spectra measurements are performed with a confocal Raman Microscope (LabRam Horiba Jovin Yvon), equipped with a notch Rayleigh rejection filter, a 600 lines mm-1 diffraction grating and a cooled CCD detector. A wavelength of 514 nm Argon and Krypton laser

(Coherent, Innova 70C series) was applied with a 40 mW power to the surfaces of these four samples with similar metallic precursor compositions, but different annealing temperature.

3.2.3 EDS and SEM

Scanning Electron Microscopy (SEM) is a powerful electron microscope technique to characterize the formed structures and produce sample surface images by scanning it with a focused beam of electrons. [46] SEM images are obtained of the CZTSe absorber surface and cross-sections without metallic coating, so the structure and thickness can be easily and quickly acquired. In this research, Hitachi Su 70 and Hitachi S800 SEM are used to characterize CZTSe absorbers.

The DEKTAK 3030 profilometer is a surface profile measuring system, which accurately measures vertical features ranging in height from 131 microns to less than 100 Angstroms on a wide variety of substrate surfaces. In this research, thickness of different layers of CZTSe thin-film solar cell devices is measured by Dektak 3030 profiometer, as a reference to the results from SEM measurement. Figure 24 shows a SEM image of the interface of molybdenum and CZTSe absorber.

Figure 24 Cross-section image of CZTSe thin-film on Mo surface annealed at 450℃

Energy-dispersive X-ray spectroscopy (EDS) is used to analysis elemental compositions of CZTSe thin-film absorbers. Each element has a unique atomic structure that allows unique set of individual peaks on X-ray emission spectrum. A high-energy beam of incident electrons is focused into the samples, and the electrons in sample materials are excited to higher energy shell, and then fall back to the lower energy shell. The energy difference between the higher-energy shell and the lower energy shell is released in the form of an X-ray. The characterized X-rays emitted from a specimen are measured by an energy-dispersive spectrometer. As the energies of the X-rays are characteristic of the difference in energy between the two atom shells and the atomic structure of emitting element, the elemental composition of the sample materials can be acquired by using EDS. An EDS graph is shown in figure 25.

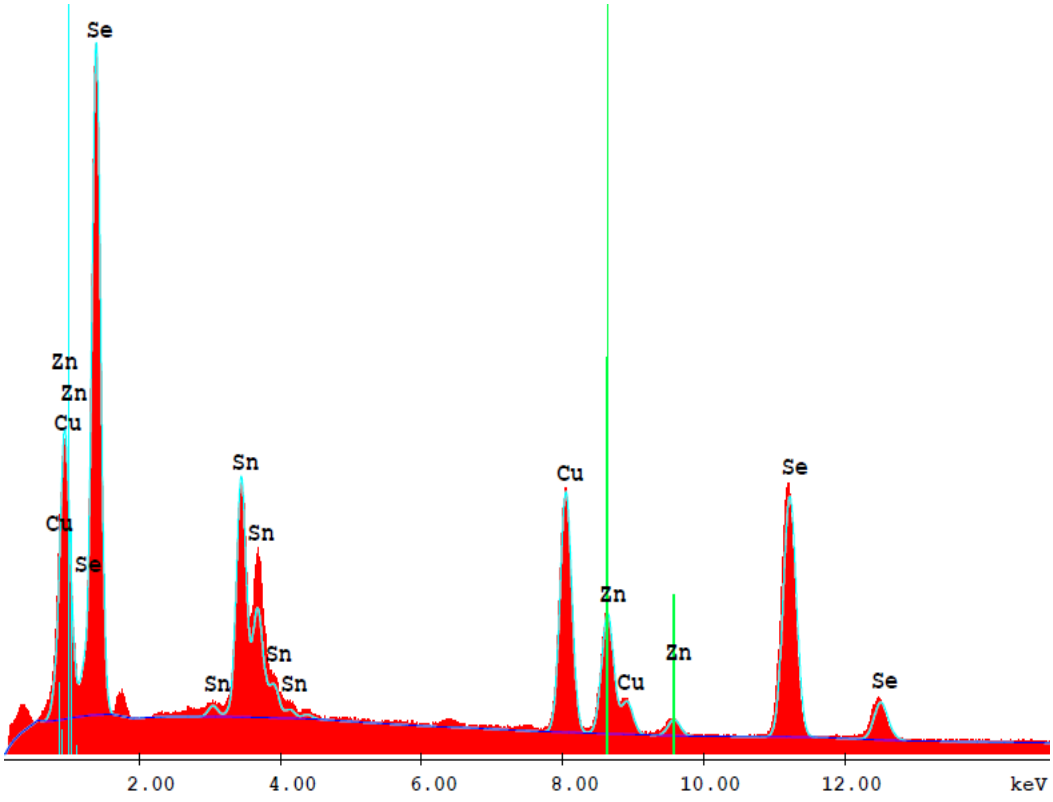

Figure 25 EDS spectrum of the CZTSe absorber

3.2.4 Spectral Response Measurement

Spectral response is the ratio of the current generated by the solar cell to the power incident on the solar cell of different wavelengths. The ideal spectral response is restricted at longer wavelengths, because the semiconductor is not able to absorb photons with energies below its band gap. Spectral response also decreases at lower wavelengths, for which photons have larger energy, and hence the ratio of current to power is reduced. Energy above the band gap of semiconductor absorber is not utilized by solar cell and instead heats up the solar cell.

An oriel cornerstone 260 monochromator was used for the spectral response measurement. The measurement is calibrated by using a standard silicon reference solar cell (calibrated by the National Renewable Energy Laboratory) for the wavelength range 400-900nm and a standard germanium reference solar cell (calibrated by the National Renewable Energy Laboratory) for the wavelength range 900-1400nm. The output current from measured solar cell device is normalized against the current of the standard across the wavelength range. Figure 26 shows a spectral response measurement plot of CZTSe thin-film solar cell device.

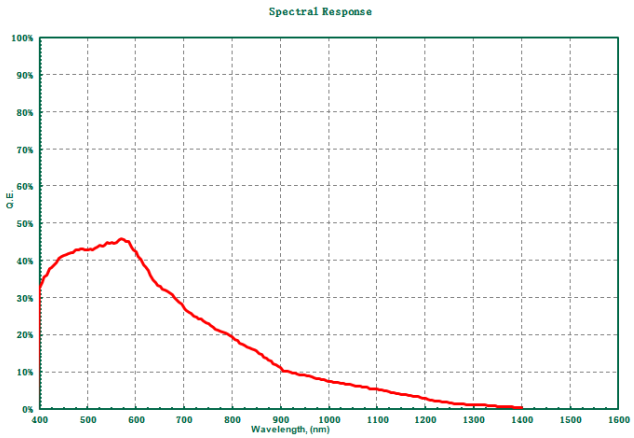

Figure 26 Spectral response measurement plot of CZTSe thin-film solar cell device

CHAPTER 4: RESULTS AND DISCUSSION

4.1 Tin Loss

Cu/Sn/Zn/Cu metallic stack precursors have been deposited onto soda-lime glass substrate in a zinc rich and copper poor condition for the sample #160, #169, #170, #175, and #180. The thickness of the first Cu layer is 20nm, the thickness of Sn layer is 330nm, the thickness of Zn layer is 290nm, and the thickness of the second Cu layer is 200nm. The stack order is designed to minimize tin loss and isolate ZnSe secondary phase from the surface of CZTSe films. The selenization time for all the samples is 30 minutes, but the selenization temperatures are different. The thicknesses of metallic stacks were measured by using

Table 5 Annealing temperatures, elemental compositions and component ratios of CZTSe films

Sample #	Annealing Temperature	Cu %	Sn %	Zn %	Se %	Zn/Sn	Cu/(Zn+Sn)	Se/(Zn+Sn+Cu)
# 160	350 °C	24.25%	13.84%	11.6%	50.31%	0.84	0.95	1.01
# 169	375 °C	25.35%	12.59%	12.91%	49.15%	1.03	0.99	0.97
# 172	400 °C	24.35%	9.69%	15.98%	49.98%	1.65	0.95	1.00
# 175	450 °C	24.98%	6.88%	18.24%	49.9%	2.71	0.99	1.00
# 180	500 °C	25.89%	3.98%	21.39%	48.8%	5.46	1.02	0.95

Dektak 3030 Surface Profiler. Elemental compositions were measured by energy-dispersive X-ray spectroscopy have been performed on Hitachi s800 unit supplied with an X-ray source and

detector equipment with an accelerating voltage of 25.0 kV and acquisition time of 60-90 seconds. And the results are summarized in Table 5, Figure 27, Figure 28, and Figure 29.

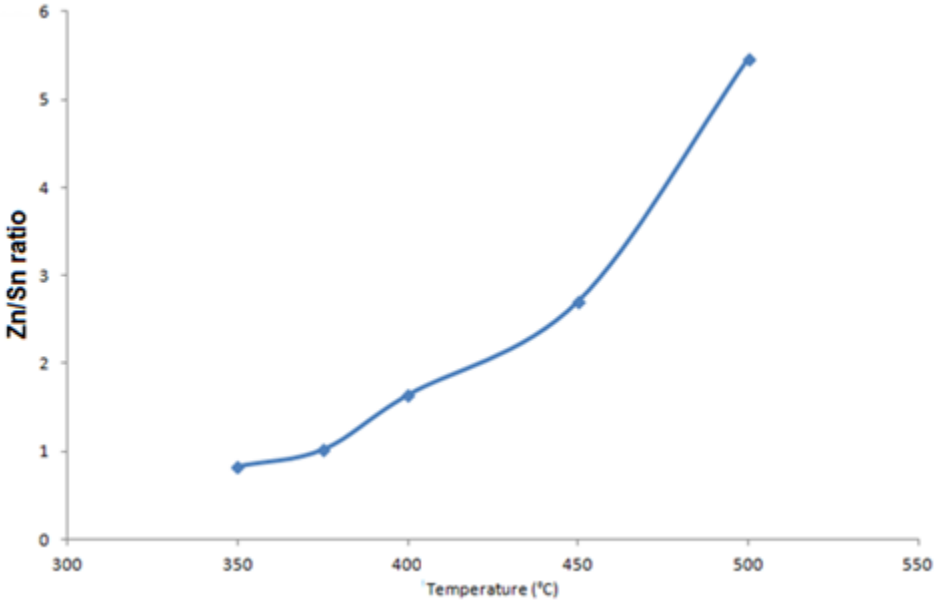

Figure 27 Zn/Sn ratio versus temperature

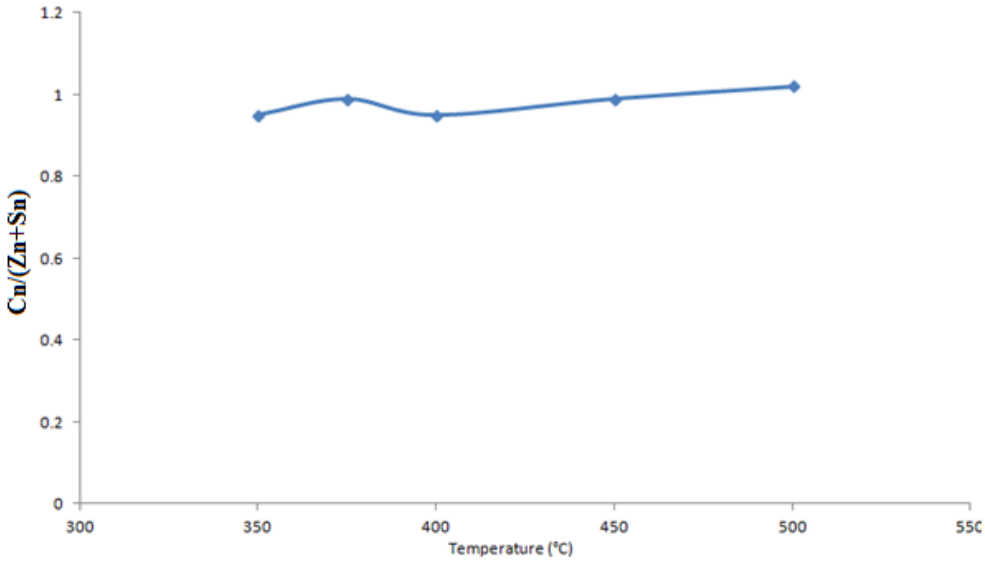

Figure 28 Cn/(Zn+Sn) ratio versus temperature

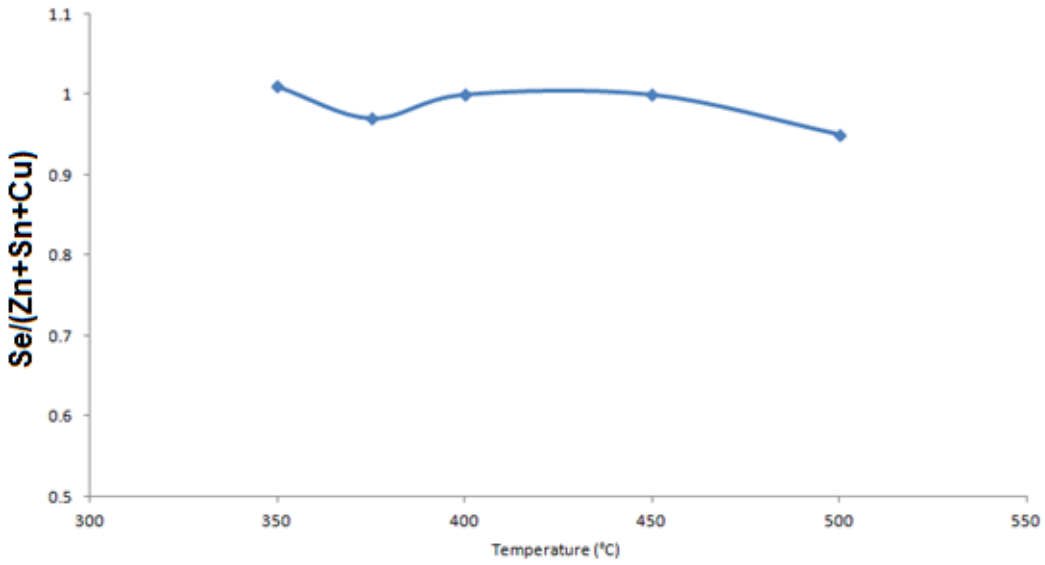

Figure 29 Se/(Zn+Sn+Cu) ratio versus annealing temperature

Zn/Sn ratio tends to increase with annealing temperature significantly. This is the clear evidence of tin loss in the samples with temperature increasing. Cu/(Zn+Sn) ratio tends to increase as well but not a lot. This indicates Zn loss occurs with annealing temperature increasing but not remarkably. Se/(Zn+Sn+Cu) ratio reduces in a small amount with annealing temperature increasing, but is still close to the stoichiometric ratio value and almost constant with annealing temperature. This implies Selenium incorporation performs as expected.

$$Sn + Se \rightarrow SnSe \quad (1)$$

$$Cu + Se \rightarrow CuSe \quad (2)$$

$$Zn + Se \rightarrow ZnSe \quad (3)$$

$$2\,CuSe + SnSe \rightarrow Cu_2SnSe_3 \quad (4)$$

$$Cu_2SnSe_3 + ZnSe \rightarrow Cu_2ZnSnSe_4 \quad (5)$$

As reported, for the reaction pathway of CZTSe system, the formations of binaries (Cu_2Se, CuSe, SnSe, and ZnSe), take place from lower annealing temperatures (220 °C). [47] [48] Sn loss happens at temperatures higher than 375 °C, and it became much more serious at higher annealing temperatures. This indicates that Sn reacted with Se and fromed SnSe at the initial stages of selenization, but the incorporation of Sn is inhibited at the beginning stage. Consequently SnSe, CuSe and ZnSe grains are formed through reaction (1), (2), and (3), and then the reaction (4) happens, which forms Cu_2SnSe_3. Hence the incorporation of Sn only happens through reacting with Cu and Se to form Cu-Sn-Se ternary as in reaction (4). Since the vapor pressure of SnSe is relatively low, Sn loss occurs in the formation of SnSe at an annealing temperature higher than 375 °C before SnSe could react with CuSe and form ternary Cu_2SnSe_3. Only in the later stage of selenization, ternary Cu_2SnSe_3 starts to react with ZnSe and form the quaternary $Cu_2ZnSnSe_4$ as in reaction (5). [52] Figure 30 shows a Cu_2SnSe_3 formed on the surface of CZTSe sample 189.

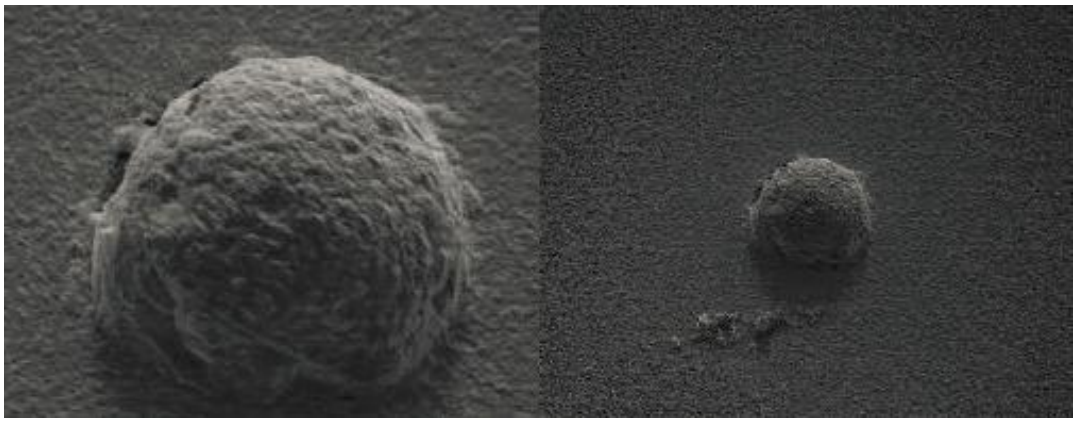

Figure 30 Image of a CuSnSe formed on the surface of CZTSe sample 189

The metallic deposition stacks order was designed to minimize the tin loss and optimize the accuracy of thickness recording through quartz crystals, because it is much easier for copper to

stick on soda-lime glass substrate surface. The Cu poor and Zn rich composition arrange was intended, because it has reached a common conclusion that Cu poor and Zn rich conditions produce devices with the best performances. Cu_2SnSe_3 is commonly known for hurting open circuit voltage, so device performances would be better off even paying the price of having secondary phase ZnSe in CZTSe absorber to avoid the formation of Cu_2SnSe_3. [27]

4.2 Detection of Secondary Phases from CZTSe Thin Films

From reported results, CZTSe single phase absorber has never been fabricated without existence of secondary phases. The major secondary phases we have encountered are ZnSe, Cu_2Se, SnSe and Cu_3SnSe_4. The presence of Cu_2SnSe_3 has been recognized as a damage of device V_{oc}, because Cu_2SnSe_3 has a band-gap around 0.82eV. It has been acknowledged that Zn rich CZTSe thin-film devices perform better than Cu rich CZTSe thin-film devices, which means the presence of small amount of ZnSe helps the device performance.

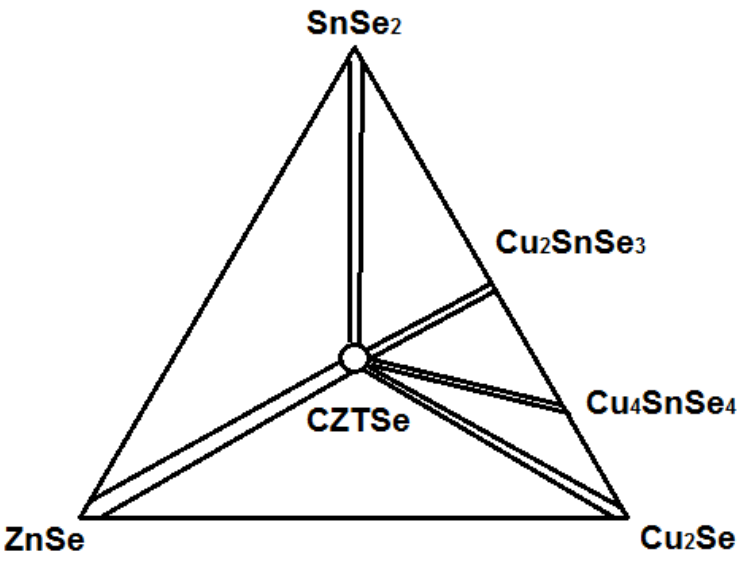

Figure 31 Phase diagram of CZTSe system

As shown in figure 31, ZnSe and Cu_2SnSe_3 overlap with CZTSe peaks in XRD measurement, so they cannot be detected from XRD. We have been using Raman scattering measurement to detect secondary phases from CZTSe thin-films. [48]

To determine the impact of both precursor composition and annealing temperature on the properties of CZTSe films, Raman spectroscopy measurement has been performed by using a confocal Raman Microscope (LabRam Horiba Jovin Yvon) equipped with a notch Rayleigh rejection filter, a 600 lines mm^{-1} diffraction grating and a cooled CCD detector. A wavelength of 514 nm Argon and Krypton laser (Coherent, Innova 70C series) was applied with a 40 mW power. In these experimental conditions, thermal effect from the laser heating is neglected. The absorption coefficient of the films at the wavelength of 514.5 nm has been determined to be about 6.2 X 10^4 cm^{-1}, which means the penetration depth of scattered light is supposed to be below 75 nm.

We had fabricated four CZTSe thin-films as below with similar compositions, but different annealing temperature, as shown in table 6. All the annealing time for four samples is 30 minutes. The Raman spectral measurements were performed on the surfaces of these four samples, and the results are shown in figure 32.

Table 6 Four selected samples with different compositions and annealing temperatures

Sample No.	Zn/Sn	Cu/(Zn+Sn)	Se/(Cu+Zn+Sn)	Annealing Temperature(℃)	ZnSe peak	Cu_2Se peak
#145	1.15	1.01	1.16	360	4.5	11
#164	1.22	0.95	1.09	420	5	2
#159	1.09	0.99	1.17	480	4	0
#178	1.16	0.91	1.23	510	0	0

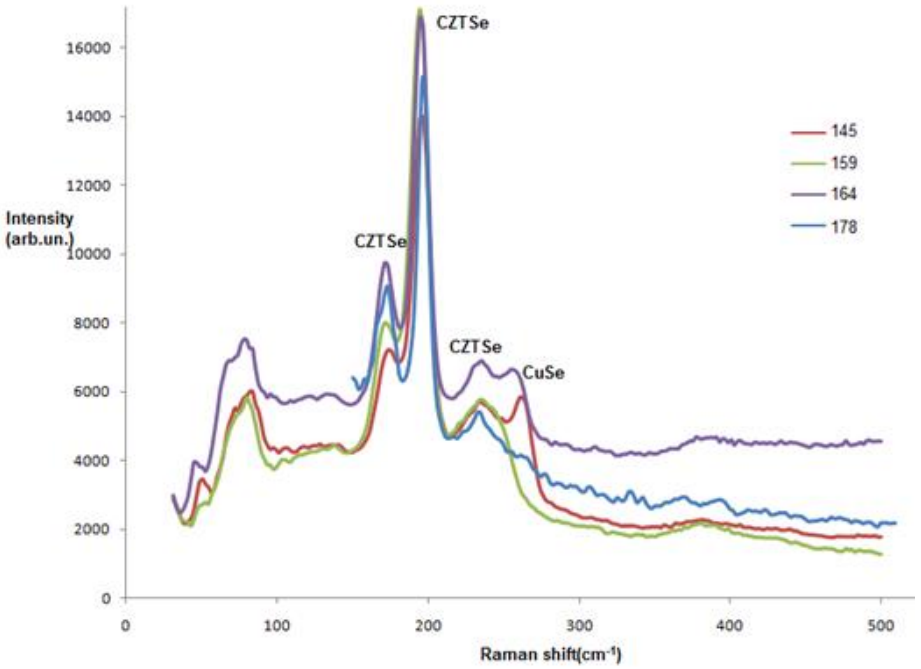

Figure 32 Raman spectrums from the four samples at different annealing temperatures

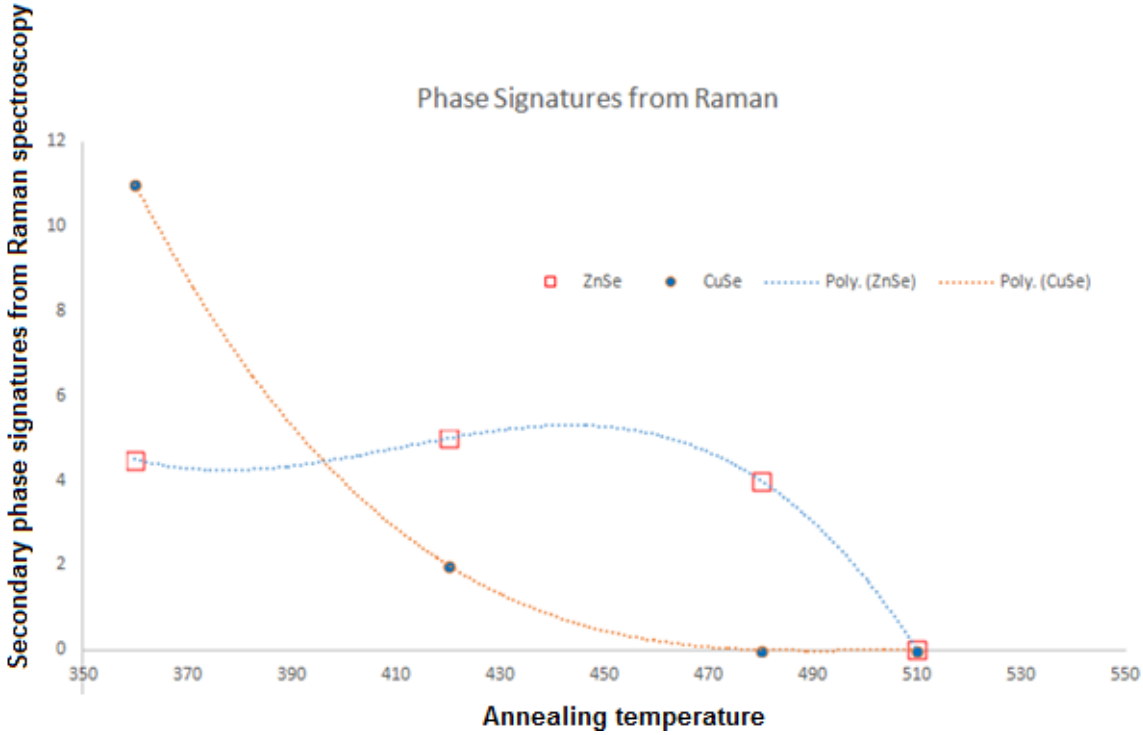

Figure 33 Secondary phase signatures from Raman spectroscopy

The major Raman peaks for all four samples represent the modes of the CZTSe quaternary compound. However the Raman spectra of sample 145 and sample164 also show evidence of the

presence of Cu_2Se at around 265 cm^{-1}. And this might be caused by uncompleted crystallization of CZTSe at lower annealing temperatures. [52] No clear ZnSe peak at 250 cm^{-1} can be seen, but the shoulder height of peaks around 250cm^{-1} for sample #164, #145, and #159 indicates the presence of ZnSe in these samples. All four samples have Zn-rich conditions, but only sample #178 doesn't show any evidence of the presence of ZnSe. This implies the formation of ZnSe on the sample surface has been inhibited at higher annealing temperature. From figure 33, we could see the trend directly, which implies the advantage of higher annealing temperature (higher than 510℃).

However, when we moved on to fabricate CZTSe thin-film devices at higher annealing temperature (higher than 510℃). We had encountered an insurmountable obstacle, which is that CZTSe films peeling off from substrate during chemical bath deposition for CdS deposition. Even when we lowered annealing time to 15 minutes and lowered annealing temperature to 420℃, the CZTSe films would always peel off from substrates during the chemical bath deposition process or ZnO deposition. This is mostly like caused by overly selenization at high annealing temperature, which leads to the formation of $MoSe_2$. The existence of $MoSe_2$ caused the bad adhesion of CZTSe film on Molybdenum surface; however we need to verify this theory. [52]

4.3 Identification of Secondary Phases at Mo/CZTSe Interface

When CZTSe thin-films has been grown on top of Molybdenum coated soda-lime glass substrate at higher annealing temperature, the CZTSe films have shown poor adhesion on the Mo/CZTSe interface. When the annealing temperature is higher than 450 ℃, the CZTSe film peeled off from the Molybdenum coated substrate, while the annealing temperature is between 420℃ to 450℃ ,

the CZTSe film didn't peel off right after selenization, but peeled off during the later chemical bath deposition process for the CdS deposition. In order to investigate the properties of CZTSe film at the Mo/CZTSe interface, we have performed the Raman scattering measurement directly on the back of CZTSe thin-film after mechanically removing the CZTSe absorber layer from the Molybdenum coated substrate. For sample 198, the annealing temperature was 450℃ for 15 minutes. After the selenization, the CZTSe film peeled off. And EDS measurement had been performed on the region, on where CZTSe film didn't peel off. The composition result shows the Zn/Sn= 1.18; Cu/(Zn+Sn)=0.9; and Se/(Cu+Zn+Sn)=1.32. After removing the CZTSe film from the substrate, Raman scattering measurement had been done on both the surface and the back of CZTSe, and the results are shown in figure 34. A SEM cross-section image was also taken with a Hittachi Su 70 as shown in figure 35.

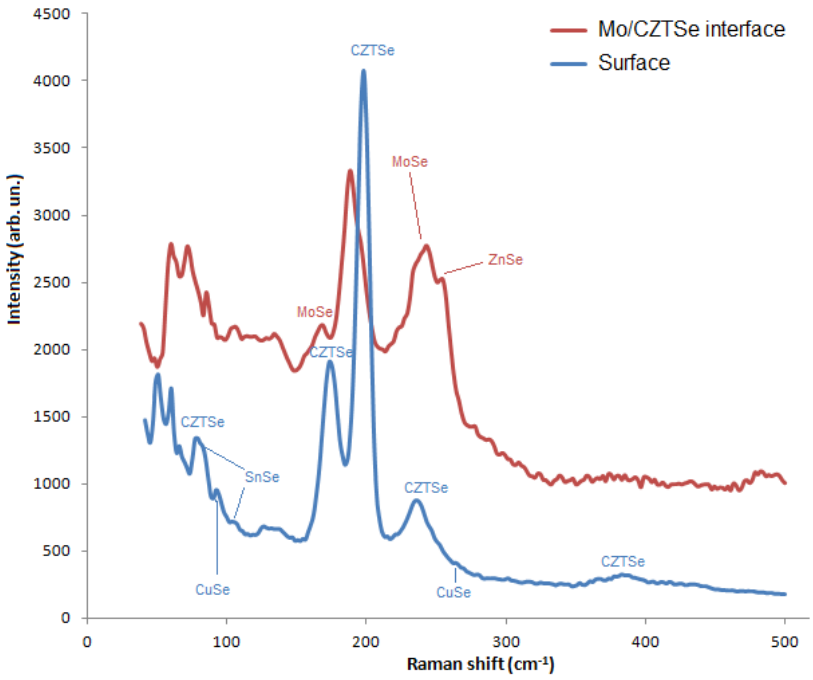

Figure 34 Raman spectra of the surface and Mo/CZTSe interface of sample 198

Figure 35 Cross-section image of sample 198 at the Mo/CZTSe interface

From the cross-section image, we could see a clear spacing at the Mo/CZTSe interface. And it happens mostly likely because the formation of $MoSe_2$ at the Mo/CZTSe interface, which has been proven from the Raman spectroscopy result. From the figure 40, we could see that, at the front surface of CZTSe film, CZTSe major peaks at 78 cm^{-1}, 172 cm^{-1}, 194 cm^{-1}, 232 cm^{-1}, and 390 cm^{-1}, can be identified clearly. A minor amount of secondary phase SnSe can be seen at peaks 80 cm^{-1} and 105 cm^{-1}, and Cu_2Se can be found at peaks 91 cm^{-1} and 261 cm^{-1}. These indicate that the formation of CZTSe compound performed well enough at the surface, with minor SnSe and Cu_2Se left on the surface, probably because of the incomplete crystallization and lack of Zn at the surface. This indicates the majority of CZTSe grain growth has always finished in 15 minutes. At the Mo/CZTSe interface, the positions of peaks present a small red-shift compared to the common values reported from literatures. [53][54] This happens most likely because of the existence of disorders and stress of the materials. [54] At the Mo/CZTSe interface, CZTSe peaks show lower intensities, we could find major peaks for ZnSe at 250 cm^{-1} and MoSe at 168 cm^{-1} and 240 cm^{-1}. And that verifies our assumption of $MoSe_2$ formation at the Mo/CZTSe interface. The formation of $MoSe_2$ at the Mo/CZTSe interface causes CZTSe films to peel off from substrates. Even the amount of $MoSe_2$ are not enough for CZTSe films to peel off,

the presence of $MoSe_2$ is well known to hurt the performances of Molybdenum back contact. Annealing at 450℃ for 15 minutes resulted in CZTSe thin-film peeling from substrate, and it implies that there is a major amount of $MoSe_2$ formed at the Mo/CZTSe interface. And this suggests us to lower the annealing temperature and time even further.

4.4 Annealing Temperature and Time of Rapid Thermal Selenization Process

We have learned that tin loss occurs significantly at 375 ℃ or higher annealing temperature for 30-mintue long selenization. On the other hand, formation of CZTSe compound performs better at higher annealing temperatures (from 500℃) , also the formation of $MoSe_2$ at Mo/CZTSe interface causes CZTSe films to peel off from substrates. After plenty of experiments, we have found out a rapid thermal selenization process that helps to solve these problems.

After the depositions of metallic precursor stacks onto molybdenum coated soda-lime glass, the sample is transferred to the second station of the reaction chamber. At 5 X 10^{-5} Torr working pressure, the selenium source is heated up to 270 ℃, which produces a selenium flux of 10 Å/S. Then graphite substrate is heated up to 220℃, at the same time, the selenium shutter is opened, the metallic precursor stacks are annealed in a selenium vapor environment and the reaction starts. The substrate temperature still goes up rapidly at a 5℃/s heating ramp to reach 375℃ , and then substrate temperature stays at 375℃ for 10 minutes. In this 10-minute period of time, it allows the binaries ZnSe and CuSe to form first, and then SnSe forms. Since this annealing temperature is not high enough for SnSe to leave rapidly, so CuSe and ZnSe could start to form Cu_2SnSe_3 before we raise the annealing temperature again. After this 10 minute annealing at 375℃, most of CuSe and ZnSe have formed Cu_2SnSe_3, with SnSe and extra ZnSe. Then we raise the annealing temperature to a higher annealing temperature (400℃-500℃) at a heating

ramp of 10 ℃ /s. At this higher annealing temperature, we stay for another period of time (5-15 minutes). The selenium source is heated up further to generate 15 Å/s selenium flux. Then we turn off the heating of selenium source and substrate, and wait for the substrate temperature to cool down to 220℃ , and then close the selenium shutter. This cooling process could take 10 minutes. This is the rapid thermal selenization process we have used, and it helps us to produce devices that are working. To find out the optimized annealing temperature and time, we have tried a range of annealing temperature, from 400℃ - 500℃, and rapid thermal selenization time 5 minutes to 15 minutes. All the samples have gone through the 10-minute initial selenization period at 375℃. I-V measurement and spectral response measurement have been performed on all the devices. The heating ramp from the initial 375℃ to the final annealing temperature is 10 ℃/S. The selenium flux is 10 Å/S for the initial selenization at 375℃, and 15 Å/S at the final annealing temperature. For all the samples, the same amounts of metallic precursors were deposited in the same Cu/Sn/Zn/Cu order. The Zn/Sn ratio is 1.18, and the Cu/(Zn+Sn) ratio is 0.91.

The annealing temperature and time for the second stage of rapid thermal selenization process and device performance parameters have been shown in table 7. From the J-V curves and the spectral response results, we could find out the best performance device is fabricated at 375℃ for 10 minutes and another 5 minutes for 450℃. For device 267 and 270, their CZTSe films peeled off during the chemical bath deposition for CdS but only partially, so we were able to carry on the fabrication on the left region on substrates.

Table 7 Different annealing temperature and time and device performance

Sample #	Annealing Temperature(℃)	Annealing time(minutes)	Isc(mA)	Voc(V)	FF	Eff
# 263	400	10+10	12.3	0.39	0.36	1.75%
#264	450	10+5	10	0.42	0.47	1.97%
#265	475	10+5	8	0.36	0.4	1.12%
#266	425	10+5	9.2	0.39	0.36	1.29%
#267	475	10+10	8.3	0.33	0.34	0.93%
#268	425	10+10	7.8	0.36	0.41	1.15%
#269	450	10+10	9.6	0.41	0.43	1.68%
#270	500	10+5	5.5	0.28	0.3	0.54%
#271	450	10+15	6.1	0.33	0.37	0.75%

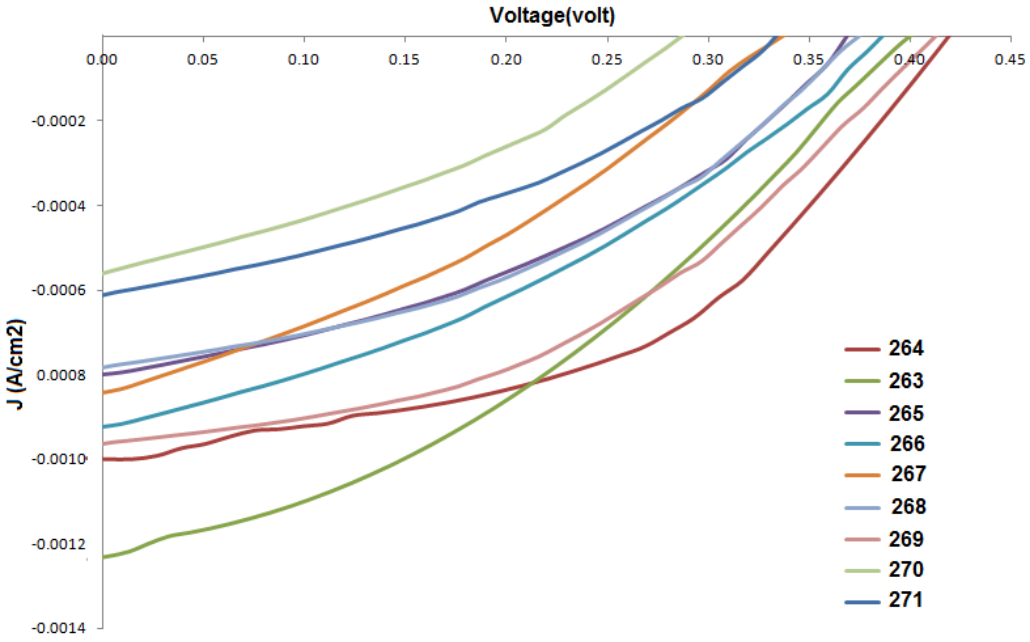

Figure 36 J-V curves for the samples of different annealing temperature and time

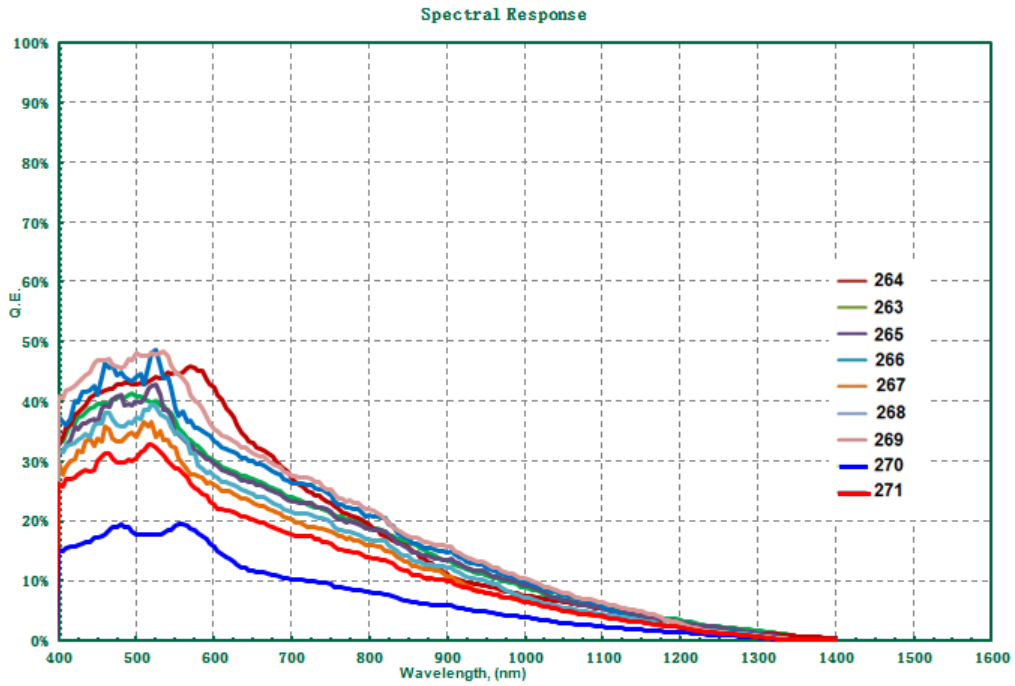

Figure 37 External quantum efficiency measurements of sample from different annealing temperatures and times

Higher annealing temperatures, higher than 475℃, is still a problem even for rapid thermal selenization process. Even part of the CZTSe films survived on the substrates and went through the rest fabrication process. However the $MoSe_2$ created at the Mo/CZTSe interface would hurt Voc, therefore impact the device performance, which agrees with the I-V curves. [55] The best open circuit voltage has been arrived is 0.42v, which is close to the Voc of the best performance CuInSe thin-film device that fabricated in our lab before. But our best short circuit current is only 12.3mA, which is main factor that brings down device performance. The low short circuit current might be caused by the presence of secondary phases in the CZTSe absorber bulk and the uncompleted crystallization of CZTSe quaternary compound. [56] And these are the trade-off from avoiding CZTSe films peeling off from substrates. As in figure 36, our best fill factor value is 0.41, this low fill factor is probably caused by the formation of $MoSe_2$ at the Mo/CZTSe interface. Because the presence of $MoSe_2$ leads to increasing series resistance, which is direct

cause of low fill factor. [57] The special response results are shown in figure 37. The most important limitation to performance is low gain due to some defect or impurities in the bulk absorber. These defects and impurities are probably caused by the uncompleted crystallization of CZTSe and the presence of secondary phases. [58] Because of the CZTSe film peeling off issue, we introduced the rapid thermal selenization process. And it allows us to achieve working devices, but the rapid selenization process would definitely leave some amount of uncompleted secondary phases in the bulk absorbers and hurt the device performance.

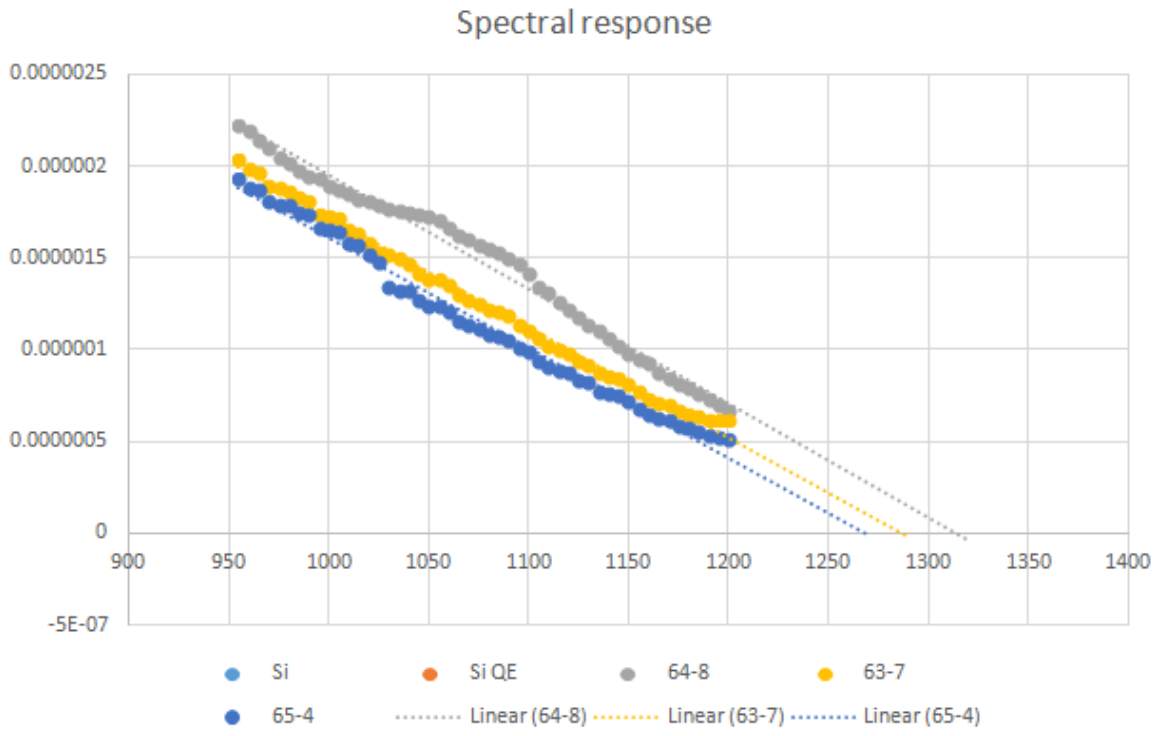

Figure 38 Band-gap determined by spectral response

In figure 38, we could estimate the band-gap of CZTSe absorber by measuring spectral response on our three samples, sample #64-8, #63-7, and #65-4, and the results are from 0.94 to 0.98eV. The band-gap of ZnSe is 2.7eV, and the band-gap of Cu_2SnSe_3 is about 0.82 eV, while the reported band-gap of CZTSe is from 0.98eV to 1.06eV, depends on the measurement techniques.

[59] Our measured band-gap results from spectral response are lower the reported values. This could imply the existence of Cu_2SnSe_3 in the CZTSe absorber bulk. Unfortunately we do not have the access to Raman spectroscopy measurement any more, we could not verify it. [60]

4.5 Precursor Stack Order Effects on Device Performance

CZTSe thin-film absorbers have been fabricated by a wide variety of techniques including physical vapor deposition, chemical vapor deposition, electroplating, and solvent and nano-particle printing. [56] The best performance CZTSe thin-film solar cell reported from literatures had involved a co-evaporation deposition and selenization process. [61] In the co-evaporation process, all four constituent elements, Cu, Zn, Sn and Se, have been deposited and selenized simultaneously. However, it is difficult to inhibit the detrimental effects of tin loss, zinc loss, and decomposition during the high temperature co-evaporation process. [61] In this research we have developed a sequential metallic stack precursor deposition process, which is separated from a later selenization process. For this stacked precursor deposition process, the order of each metallic layer has played a significant impact on the film properties and device performance. Herein this sequential metallic stack deposition process also offers us plenty of room to manipulate the procedure, in order to optimize the CZTSe film properties and improve device performance. [61][62]

To investigate the influences of precursor stack order on the device performance, we have fabricated three devices by following three different precursor stack orders, however the total thickness of each metallic precursor layer are constant as shown in Table 8. The CZTSe film compositions have been measured by using EDS separately and later three devices have been

fabricated and characterized with I-V measurement and spectral response. The results are shown in figure 39 and 40.

Table 8 Precursor stack orders and device performance parameters

Sample #	Precursor order	Zn/Sn	Cu/(Zn+Sn)	Isc	Voc	FF	Eff
# 264	Cu(10nm)/Sn(320nm)/Zn(270nm)/Cu(200nm)	1.16	0.91	10mA	0.42V	0.47	1.97%
# 272	Cu(210nm)/Sn(320nm)/Zn(270nm)	1.01	0.98	4.8mA	0.24V	0.29	0.34%
# 273	Sn(320nm)//Zn(270nm)/ Cu(210nm)/	1.23	0.95	7.5mA	0.36V	0.41	1.11%

From the EDS composition results, we could see the metallic precursor order has a significant influence on the CZTSe film composition. And these effects on film composition also play a role on the device performance differences. In the experiments, metallic precursor stacks depositions have been carried out with thermal evaporation method by following different stack orders. From the EDS results, we could see the Zn/Sn ratio for sample #272 is much lower than #264 and #273, and zinc was deposited on the very top of all the stacks. So during the selenization process, the top layer of zinc would partially evaporate before reacting with selenium and forming ZnSe. Correspondingly the Zn/Sn ratio from sample #264 is close to the expected value, which means zinc had not lost significantly during the selenization process, probably because there is a thick copper layer on top of zinc. The top Cu stack reacted with selenium right away at the beginning period of selenization process, and the formed CuSe layer inhibits zinc loss. From sample #273, we could see the highest Zn/Sn value from sample #273, probably due to the bad adhesion of tin on molybdenum surface, we deposited less Sn than we expected. From our past experience, we found out both Sn and Zn have adhesion issues on molybdenum surface at the beginning of deposition, and we have not observed any adhesion problem of Cu on molybdenum surface. That is why in sample # 264, we have deposited a very thin layer of Cu (10nm) on the molybdenum

coated substrate. Therefore Sn and Zn could have better adhesion on during their deposition processes. With a thick layer of Cu on top of the metallic precursor stacks, zinc loss and SnSe loss during the selenization process can be effectively inhibited. This allows us have a better control of the CZTSe thin-film composition. Also Zn is found to be detrimental as the lowest layer, because the formation of large amount of ZnSe at the bottom region of absorber has a negative effect on device performance. [63]

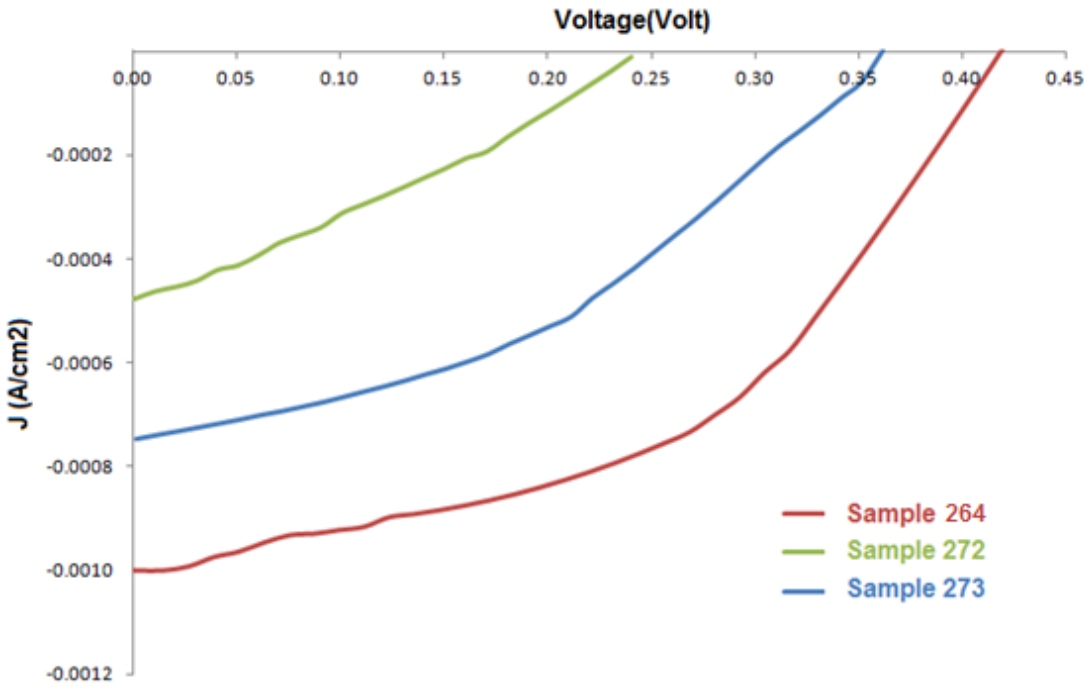

Figure 39 Illuminated AM1.5 J-V curves with different metallic precursor stacks orders

From the J-V curves and spectral response results, we could see that the Voc of device #272 is significantly low, and this might be caused be zinc loss at the beginning of selenization process, which leads to extra Cu and Sn in the absorber bulk, so extra Cu_2SnSe_3 is left in the absorber bulk.

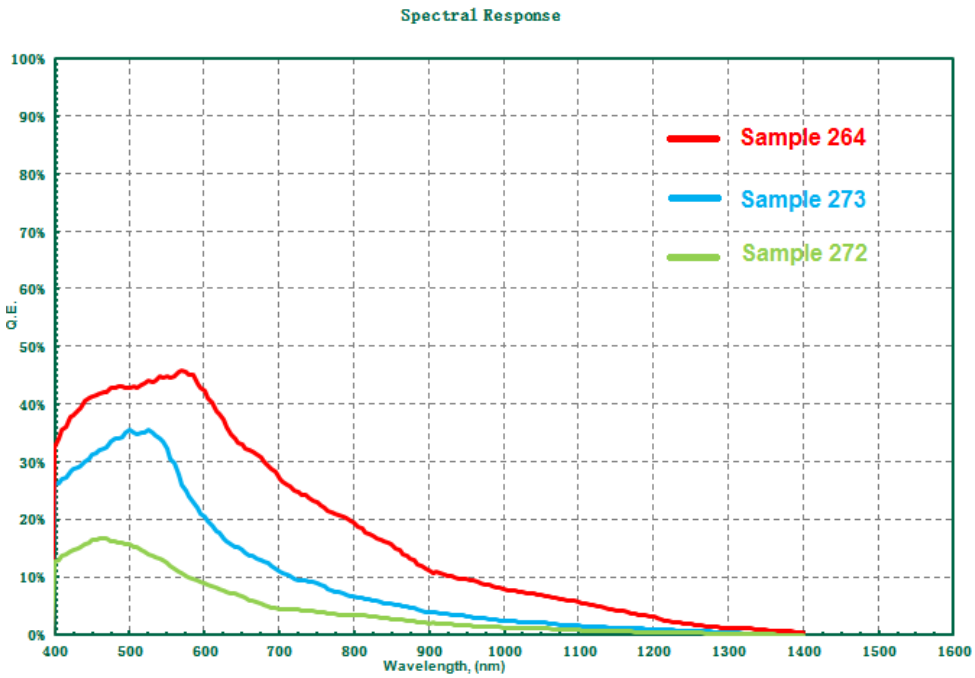

Figure 40 External quantum efficiency measurements of three samples with different metallic precursor stacks orders

Cu_2SnSe_3 is well known for hurting the device Voc. For device #273, due to the bad adhesion of Sn on molybdenum surface, we deposited less Sn than we expected. So there are extra Zn and Cu left in the absorber, which would form secondary phases CuSe and ZnSe. These secondary phases hurt both Voc and Isc, as can be seen from the I-V curve. And the spectral response results also agree with the I-V measurement results. Also Sn at the bottom of the metallic stacks, could cause the formation of SnSe at the bottom of absorber, and this may reduce the current collection at higher wavelength range and hurt fill factor. [64] And this can be verified from the spectral response result. Therefore, we have found out the best performance device is followed a Cu/Sn/Zn/Cu metallic precursor stack order. A thick layer of Cu is on top of Zn and Sn could help to minimize tin loss and zinc loss during the selenization process. In this way, we could control the CZTSe thin-film composition better, and reduce the possible secondary phase existence in the CZTSe thin-film. Also the formation of CZTSe quaternary compound could

perform relatively completely, which benefits the device performance. Incomplete formation of CZTSe could cause the formation of Cu_2SnSe_3, which hurts the Voc, as shown in the J-V curves. Also since Cu has better adhesion properties on the Molybdenum surface than Sn and Zn by depositing a thin layer of Cu on Molybdenum first helps to control the stoichiometry. [64]

4.6 Influence of CZTSe Composition on Device Performance

Metallic precursor composition plays a crucial role in properties of CZTSe film. As we have known, due to the well known fact that Cu_2SnSe_3 hurts open circuit voltage, all the reported best performance CZTSe devices are in Zn-rich and Cu-poor conditions. Since the existence of ZnSe inhibits the formation of Cu_2SnSe_3. Since we know the fact that by using our rapid thermal selenization process the CZTSe grain growth cannot be complete, there have to be some secondary phases that exist in the CZTSe absorber bulk. This is the trade off for not to having formation of MoSe at Mo/CZTSe interface which causes fatal CZTSe film peeling off from substrate. In order to minimize the drawbacks of uncompleted CZTSe crystallization and existence of secondary phases, we have tried to optimize the CZTSe component composition, to figure out the most suitable composition configuration that could maximize the device performance by using our rapid thermal selenization process.

To investigate the influence of CZTSe composition on device performance, we have fabricated six samples with different metallic compositions. EDS was used to determine the composition, while the thicknesses of all samples are about 800nm, and the J-V measurement and spectral response measurement have been performed on these samples to test device performance. The composition values and device performance parameters are shown in table 9, I-V curves are shown in figure 41, spectral response results are shown in figure 42, and we also concluded the

Voc tendency over Cu/(Zn+Sn) value and fill factor tendency over Isc in figure 43 and figure 44. [64]

Table 9 Device performance with different metallic precursor compositions

Sample #	Zn/Sn	Cu/(Zn+Sn)	Isc(mA)	Voc(V)	FF	Eff
#275	1.19	1.11	5	0.24	0.31	0.37%
#276	1.11	1.03	7.9	0.36	0.42	1.19%
#277	0.92	0.99	6	0.31	0.32	0.6%
#278	0.99	1.06	8	0.34	0.32	0.87%
#280	1.22	0.83	9.3	0.39	0.41	1.45%
#282	1.17	0.75	5.6	0.34	0.37	0.75%

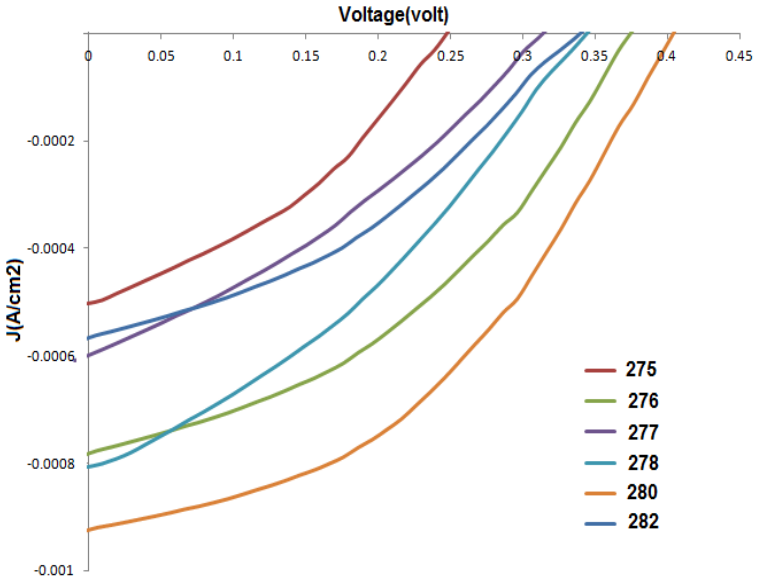

Figure 41 J-V curves for the samples with different metallic precursor compositions

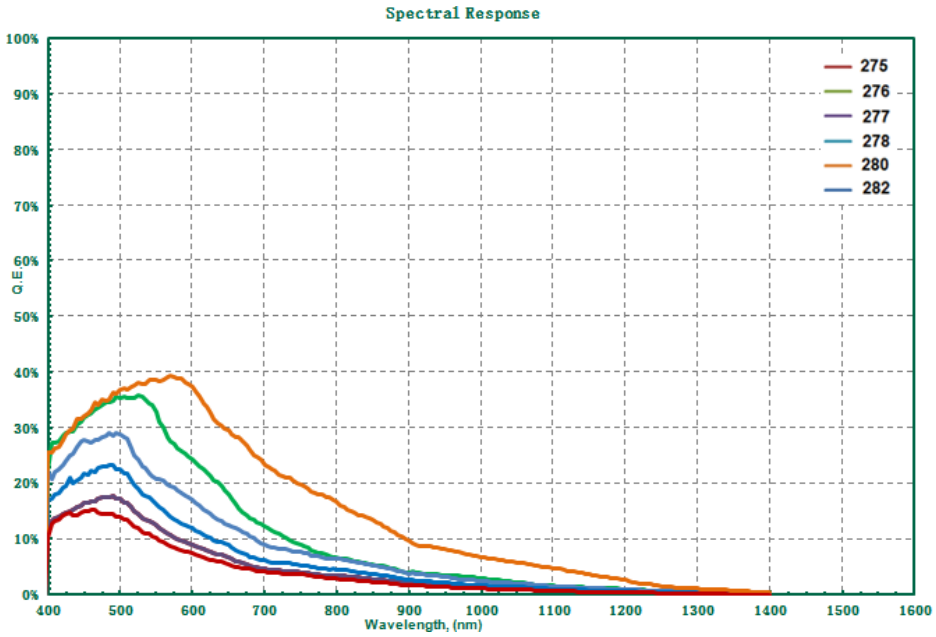

Figure 42 External quantum efficiency measurements of samples with different metallic precursor compositions

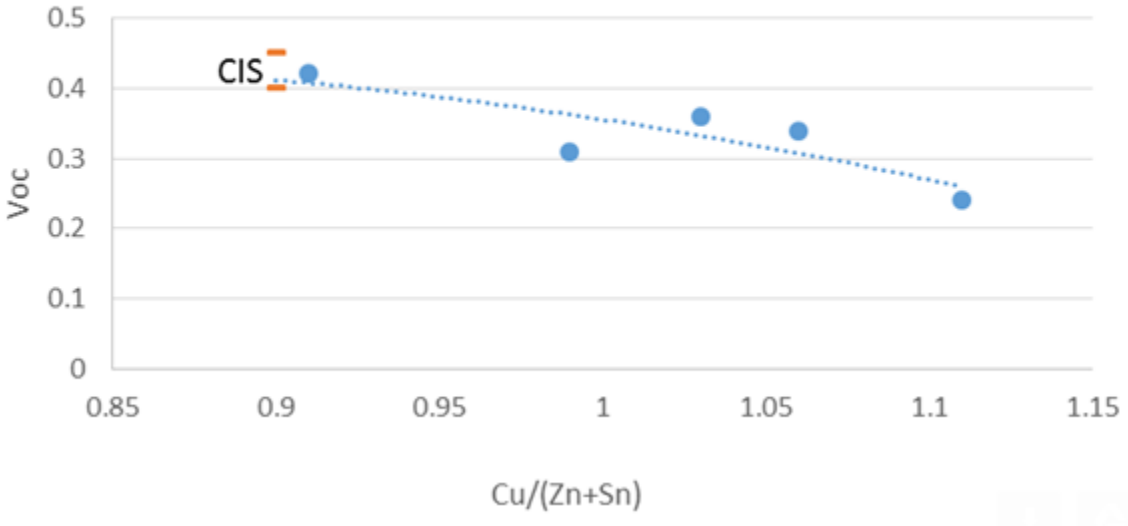

Figure 43 Voc tendency versus Cu/(Zn+Sn) value at 450 ℃

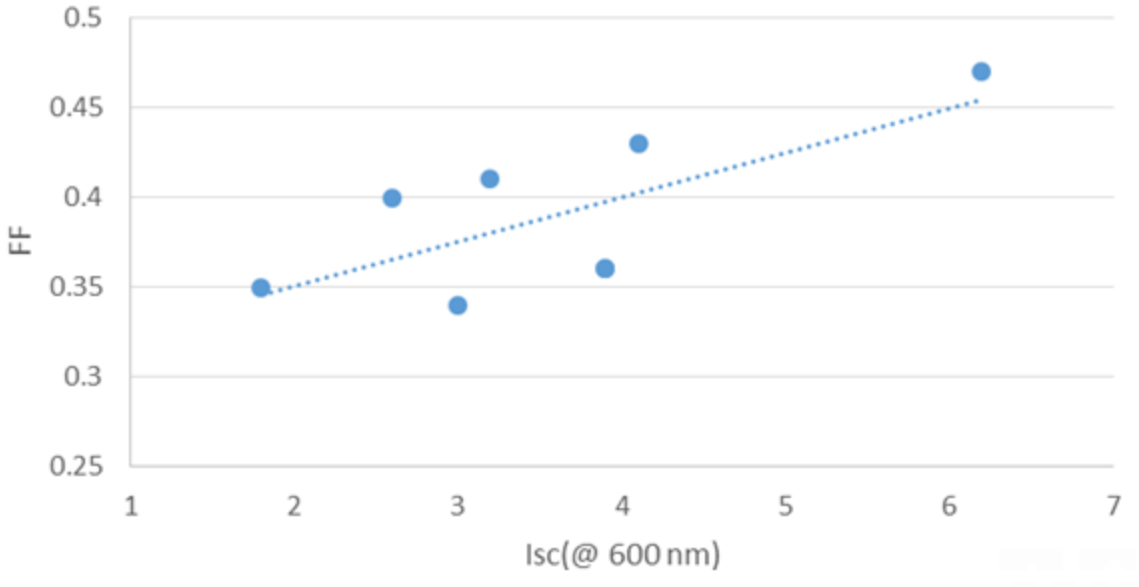

Figure 44 Fill factor tendency versus Isc at 600nm

As we expected, from the J-V curves and spectral response results, we could see the best performance device has the Cu-poor and Zn-rich composition. However, too much extra Zn would definitely hurt the device performance. The best performance CZTSe device reported from literatures has a composition of Zn/Sn= 1.19, Cu/(Zn+Sn)= 0.92. To get more accurate Isc value of our devices, we have integrated the current value across the entire available wavelength range in spectral response, and the best Isc we have is 14.5mA, this increases our best performance device efficiency to 2.86%. Since our spectral response measurement setup needs to be calibrated every time from reference and the band-gap of CZTSe is about 0.9-1eV. In order to measure spectral response on our CZTSe films across the entire available wavelength range, we need to use germanium or other materials have a lower band-gap as reference. From the figure 49, we could see the Voc is relatively constant over Cu/(Zn+Sn) ratios. The best Voc we have achieved is 0.42V. It is close to the Voc value of CuInSe thin-film solar cell devices that we have fabricated before by using the similar fabrication processing steps in our lab. As long as there is

no major amount of Cu_2SnSe_3 present in the CZTSe absorber bulk, the Voc value is relatively constant, in a range from 0.35V to 0.42V range.

From the figure 50 and I-V curves, we could conclude that both Isc and fill factor of our devices are fairly low, they are the major issues that deteriorate the performance of our devices. The reason why Isc and FF are limited could comes from the same loss mechanism. While the presence of $MoSe_2$ at Mo/CZTSe interface deteriorates the fill factor by increasing device series resistance, this should not have a major effect on Isc. As reflected from spectral response results, we have found out the most important limitation to performance is low current gain, maybe due to some defect or impurities in the CZTSe bulk absorber. And also the annealing temperature has an effect on the Isc, so the defects in the CZTSe bulk absorber most likely have played a role in the low current gain issue. Moreover we have fabricated plenty of CZTSe thin-film absorbers with visible pinhole on the surface. We could conclude small pinholes do exist in our CZTSe absorber bulk, and the pinholes indicate the existence of defections. The cause of pinholes could be the impurities from the soda-lime glass substrates, since the soda-lime glass substrates we have been using are normal store bought products and they are not well quality controlled. Various impurities from the glass substrate could cause pinholes in our CZTSe absorber bulks. And the rapid thermal selenization process we have developed would most likely leave uncompleted secondary phases in the CZTSe absorber bulks, since the reaction time is in the short range. For instance, since the Sn was deposited right on top of the most bottom thin Cu layer, so if there is SnSe formed at the Mo/CZTSe interface, this also would reduce the current collection at higher wavelength range and deteriorate fill factor. And this can be verified from the spectral response results on our devices. To avoid the presence of Cu_2SnSe_3, which hurts Voc of devices, we have fabricated devices in Zn-rich conditions. And this means extra ZnSe must

exist in our CZTSe bulk absorbers. And the drawbacks of Zn excess on CZTSe device performance have been reported to be highly conditional upon the location of ZnSe in CZTSe bulk. [65] The segregation of ZnSe at the back contact of the device is neutral on the influences of device performance, due to relatively low minority carrier diffusion lengths. However, ZnSe on the surface of CZTSe bulk absorber could deteriorate the device performance significantly. ZnSe formed at the surface of CZTSe bulk absorber causes major problems to the PN junction, it hurts the Isc, as well as the Voc and fill factor. The possibility of existence of ZnSe on the surface of CZTSe bulk cannot be eliminated in our devices, since our rapid thermal selenization process time is fairly short. With a Zn-rich condition, it is possible to have ZnSe left at the surface of CZTSe bulk. This possible ZnSe presence on top of CZTSe bulk could block the photo-generated current coming from underneath ZnSe. If this is really happening in our devices, then it definitely would hurt the Isc and deteriorate the current collection as showing in the spectral response measurements.

CHAPTER 5: CONCLUSIONS

CZTSe thin-film solar cells have shown a promising perspective as an alternative to currently more mature thin film technologies such as CIS, CIGS, and CdTe, because they are only composed of earth abundant and non-toxic elements.

In this research, we have focused on fabrication of CZTSe thin-film solar cell devices with mass production friendly technique. We have also developed a sequential metallic precursor stack deposition process and a two-step rapid thermal selenization process, which could reduce the presence of secondary phases.

Tin loss mechanism has been studied at the beginning of this research. We have found out that tin loss during selenization annealing process happens at 375°C or higher annealing temperature. Tin loss is happened in a form of SnSe, and SnSe has a relatively low vapor pressure. We also found out that zinc loss happens as well at the beginning stage of selenization process. Zinc loss happens because zinc is highly volatile in high vacuum at a relatively low reaction temperature. However, through our rapid thermal selenization process, zinc loss is not as a serious issue as tin loss. Tin loss has a significantly influence on the properties of CZTSe thin-films. Extra secondary phases, such as Cu_2Se and ZnSe could remain in the CZTSe absorber bulk, which deteriorate the properties of CZTSe thin-films. Zn loss happens during the selenization process, because of the high annealing temperature. Zn loss from the CZTSe absorber bulk leads to the break of thin-film stoichiometry. And Cu_2SnSe_3 formed by extra Cu and Sn due to Zn loss, deteriorates the open-circuit voltage significantly. Since most likely possible Zn loss would

happen at the top of the CZTSe absorber bulk, which is at center the P-N junction, it may help the device performance significantly.

The existence of secondary phases in CZTSe absorber bulk has always been a major issue for this semiconductor material. Actually single phase CZTSe absorber has never been fabricated without presence of any secondary phases. However, the presence of certain secondary phase is not necessarily a drawback. For instance, the existence of ZnSe in the CZTSe absorber bulk could effectively inhibit the formation of ternary Cu_2SnSe_3, which is well acknowledged as hurting the open-circuit voltage of device. The major secondary phases we have encountered are ZnSe, Cu_2Se, SnSe and Cu_2SnSe_3. We have found out that, during the selenization process, binaries ZnSe, Cu_2Se, and SnSe form first at the beginning of the selenization process, then later Cu_2Se and SnSe react and form Cu_2SnSe_3. In the later stage of selenization process Cu_2SnSe_3 and ZnSe start to react and form $Cu_2ZnSnSe_4$. And at certain condition, crystallized $Cu_2ZnSnSe_4$ could also decompose. ZnSe and Cu_2SnSe_3 overlap with CZTSe peaks in XRD measurement, so they cannot be detected from XRD characterization. We have been using Raman spectroscopy measurement to detect secondary phases from CZTSe thin-films. And from the Raman spectroscopy result analysis, we have found out that higher annealing temperature (higher than 510℃), produces better crystallized CZTSe thin-film grains, with less secondary phases.

However, in the later device fabrication, we have found out that higher annealing temperature brings upon a crucial insurmountable obstacle, which is newly fabricated CZTSe thin-films absorber layers peel off during the later chemical bath deposition process of CdS deposition. From Raman spectroscopy characterization, we verified our assumption, which is the formation of $MoSe_2$ at Mo/CZTSe interface causes the CZTSe thin-films peeling off from substrates during chemical bath deposition process. In order to avoid this issue from happening, we have to lower

the selenization annealing temperature and time. According to our finding of tin loss happens at 375°C and higher annealing temperature. After plenty of experiments, we have developed a rapid thermal selenization process for our fabrication of CZTSe thin-film solar cell devices. It solved the problem of CZTSe thin-film peeling from substrate. Because this rapid thermal selenization process lowered the annealing temperature and time, it ineluctably causes the presence of uncompleted CZTSe grain growth and secondary phases remaining in the CZTSe absorber bulk. This is the trade-off on avoiding CZTSe thin-film from peeling off substrate. This rapid thermal selenization process includes two steps of selenization, the first step of selenization happens at 375°C for 10 minutes, in a selenium vapor environment with selenium flux is 10 Å/s. Then the annealing temperature is raised up to 450°C at a heating ramp of 10°C/s. The second step of selenization happens at 450°C for 5 minutes.

Since we know the drawback of this rapid thermal selenization process is to have secondary phases remain in the CZTSe absorber bulk. More research about optimizing the metallic precursor stacks deposition process has been done, in order to minimize the existence of secondary phases. And we have found out that the metallic precursor stacks order has played an important role in the device performance. Several configurations of metallic precursor stack order have been tried out. From the results, we have designed a special stack order, Cu/Sn/Zn/Cu, which has been proven to optimize the device performance.

Secondary phase formations at the surface of CZTSe films and the Mo/CZTSe interface have been also studied via Raman spectroscopy measurement. ZnSe that exists at the top of CZTSe absorber bulk deteriorate device performance by blocking the current collection coming from underneath, and this would hurt current collection performance on spectral response result.

However ZnSe at the back of CZTSe would not do as much harm as ZnSe at the top of CZTSe absorber.

We have also studied the influence of elemental composition on the device performance. And the results agree with the reported result, Cu-poor and Zn-rich conditions have proven to have great advantages on device performance, probably because it avoids the presence of Cu_2SnSe_3. The best performance device we have fabricated has 2.86 % efficiency, with a 0.42 Voc, 14.5 mA/cm^2 current density, and 47% fill factor.

Further research needs to be done on characterization of secondary phases and their influence caused by this rapid thermal selenization process. And a buffer layer could also be introduced at the Mo/CZTSe interface to reduce the crucial influence of $MoSe_2$.

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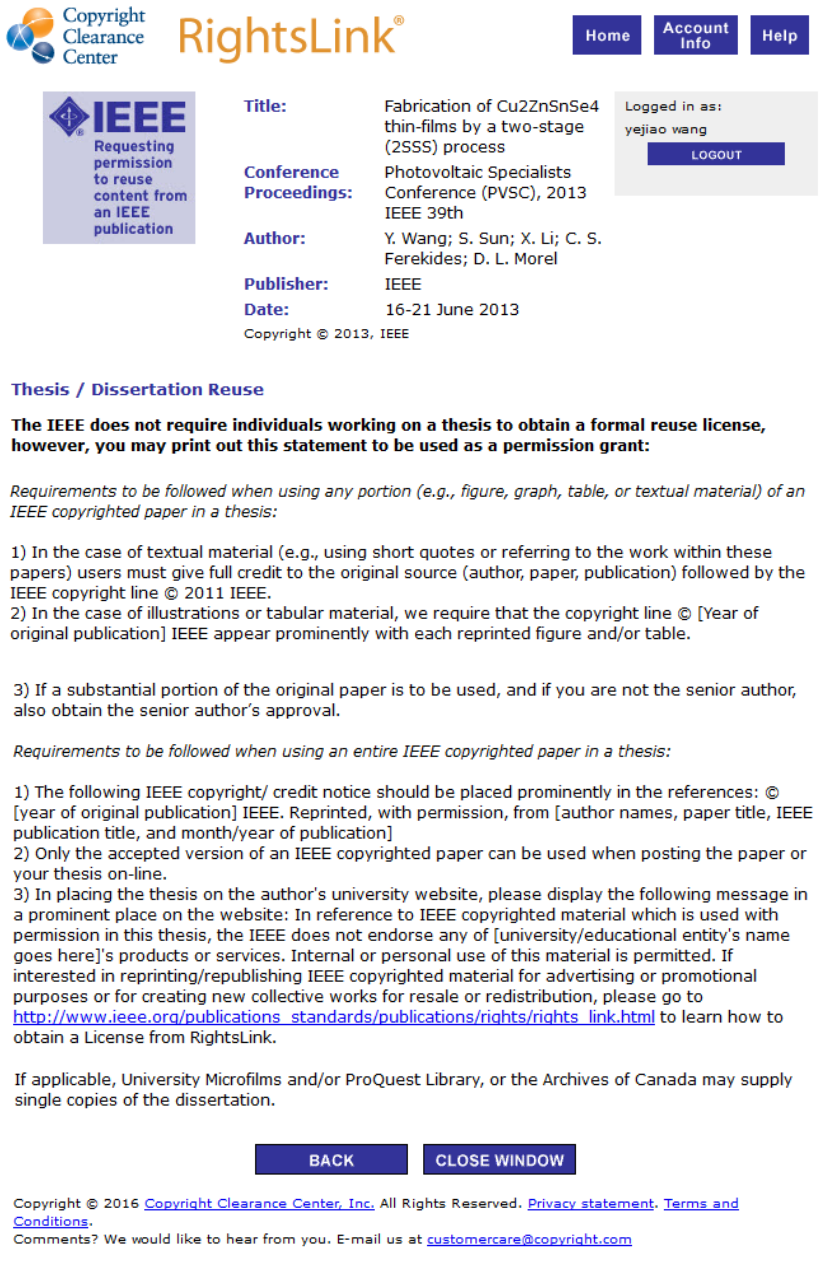

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